TIGER: A front-end ASIC for timing and energy measurements with radiation detectors

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Abstract

A mixed-signal ASIC for timing and energy measurements with radiation detectors is presented. The chip embeds 64 channels, each of which features a charge-sensitive amplifier followed by a dual-shaper coupled to low-offset discriminators. A versatile back-end, incorporating low-power Time to Digital Converters and Wilkinson Analog to Digital Converters with derandomizing buffers allows to encode both the time of arrival and the charge of the input signal. The ASIC is designed for a maximum detector capacitance of 100 pF and an event rate in excess of 60 kHz per channel. A peak detector samples the input signal with an excellent linearity in the range $1 \div 50$ fC. Charge digitization with Time-over-Threshold is also supported to extend the dynamic range. Fabricated in a 110 nm CMOS process, the chip dissipates 10 mW/channel. The ASIC was primarily developed to readout the cylindrical GEM detector of the BESIII experiment. For its characteristics it can serve however a broad class of radiation sensors, including silicon microstrip detectors.

Keywords: `elsarticle.cls`, LaTeX, Elsevier, template

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1. Introduction

TIGER (Turin Integrated GEm Readout) is a 64-channel mixel-signal ASIC that allows simultaneous time and energy measurements with radiation detectors. The chip has been primarily developed to readout the Cylindrical Gas Electron Multiplier detector (CGEM), a novel ultra-light weight tracker to be installed in the inner part of the BESIII experiment, a tau-charm factory exploiting the Beijing e^+e^- collider BEPCII [1].

The CGEM detector is formed by three independent concentric layers, covering 93% of the solid angle. Each layer is in turn composed by five cylindrical structures: one cathode, three GEM foils and the readout anode. One GEM foil is made of a layer of 50 μm Kapton, copper clad on each side and with a high density of bi-conical holes. The holes have an inner diameter of 50 μm and an outer diameter of 70 μm. Inside each hole, an electric field of 100 kV/cm multiplies the number of primary electrons to achieve a detectable signal. The triple GEM structure is chosen because it allows to reach high gain with a minimum discharge probability.

Embedded in a 1 T magnetic field, the new tracker must provide a momentum resolution of 0.5% at 1 GeV and a rate capability of 10 kHz/cm^2 . A spatial resolution of 120 μm in the direction transverse to the beam and of 1 mm in the longitudinal one is targeted. The total radiation length must be below 1.5%. A readout pitch of 650 μm coupled with charge interpolation has been chosen to limit the total number of front-end channels to 10.000. The anode capacitance can be up to 100 pF, while a typical signal is expected to range from 3 fC to 50 fC. To improve upon the spatial resolution on angled tracks, it is foreseen to operate the detector in the so-called "micro-TPC" (μ-TPC) mode. This requires that each hit is also time-tagged with a good time resolution. Fig. 1 shows a conceptual design of the detector. Further technical details can be found in [2, 3].

The relevant specifications for the CGEM front-end electronics are summarized in table 1.

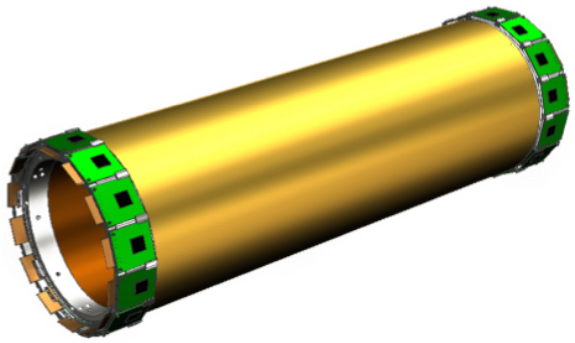

Figure 1: Concept of the CGEM detector.

Input Charge	1-50 fC
Input Capacitance	Up to 100 pF
Data Rate	60 kHz/ch
Non-linearity	$< 1\%$
Charge Collection Time	60 ns
Power Consumption	$<$10 mW/ch
Technology	110 nm process

Table 1: Design specifications of the TIGER chip.

The limited space available to host the front-end cards at the tracker edges calls for a compact and robust design. A mixed-signal ASIC was thus developed on purpose for the project. Fabricated in a 110 nm CMOS technology, the chip integrates in an area of 5 mm $\times$ 5 mm 64 parallel channels that extract and digitize the amplitude and time-of-arrival of the input signal. To allow proper grounding and minimise interference noise, any relevant signal processing task is performed on chip and the ASIC communicates with the external environment using only digital low-voltage differential signalling (LVDS). The TIGER ASIC is composed by two main functional units. The first one, the very front-end, amplifies and shapes the input signal and has been optimized to carefully match the requirements of the CGEM detector. The second, called "back-end" in the following, includes the time and amplitude digitizers along with the digital

control logic. This part has been kept as flexible as possible in order to favour its re-use in different projects. This approach will allow in fact to develop in a short time a new ASIC in which only the very front-end is changed to allow its throughout optimization to a particular kind of radiation sensor. The chip architecture is described in more detail in Section 2 and experimental results are reported in Section 3.

2. ASIC architecture

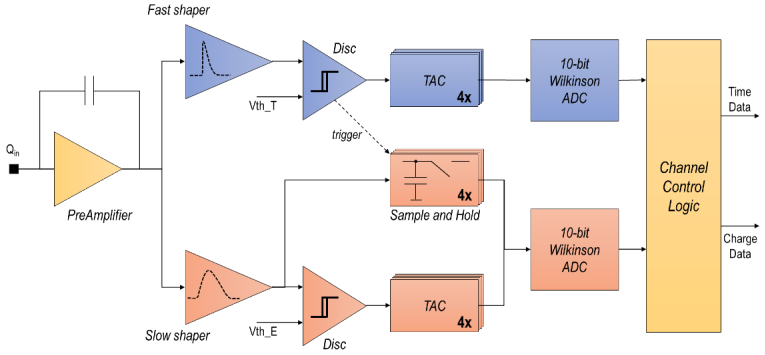

Figure 2: Block diagram of one ASIC channel.

Fig. 2 shows the block diagram of one processing channel. The input stage amplifies the detector current and feeds two independent continuous-time shapers. In the fast shaper the peaking time is matched to the expected charge collection time (60 ns) with the purpose of providing optimal timing performance. The peaking time of the slow shaper is chosen to be 170 ns in order to improve the charge resolution while keeping a good event rate performance. In the preamplifier and in the shaper class AB single-ended amplifiers are employed [4, 5]. Each shaper is followed by a voltage-mode discriminator, whose threshold can be fine-tuned on a channel-by-channel basis with a dedicated 6-bits DAC. Two low-power TDCs are provided in each channel. The coarse time information is obtained by counting the transitions of the chip master clock, that can be up to 200 MHz. A Time-to-Amplitude Converter (TAC) is employed to interpolate

the time elapsing between the hit detection flagged by the discriminator and a suitable clock edge. The analogue voltage of each TAC is then digitized by a Wilkinson ADC with a maximum resolution of 10 bits. To make the interpolation robust against metastability in the digital logic, a time corresponding to 1.5 the master clock period is measured, therefore a theoretical minimum binning of 7.3 ps is possible. Increasing the time bin reduces the conversion time accordingly. For instance, measuring the interpolation time with a 7 bit resolution results in a binning of 60 ps and a maximum conversion time of 640 ns. Four TACs are available for derandomization purposes [6, 7], therefore the TDC can accommodate an event rate in excess of 1 MHz with an efficiency better than 99%. Rate capability is thus mainly limited by pulse pile-up in the front-end amplifier. An array of four capacitors allows to sample and hold the peak voltage at the output of the slow shaper. The stored voltage is digitized by a second Wilkinson ADC, which is shared with the TDC serving the energy branch.

The chip operation is supervised by a digital controller [8, 9]. This unit generates all the digital signals necessary to drive the S&H, the TDC and the Wilkinson ADC and manages the chip configuration and the data transmission to the outside world. Each hit generates a 64 bits word, which can be transmitted over one of the four serial LVDS links in 32 clock cycles thanks to the Double Data Rate (DDR) operation. With a clock frequency of 200 MHz, the total output bandwidth is 1.6 Gbit/s. This allows to transmit $2.5 \cdot 10^7$ events/s, which is equivalent to a frequency of 390.625 kHz/channel. Triple Modular Redundancy (TMR) is employed to protect critical registers against Single Event Upsets (SEU).

Thanks to the hardware resources deployed in each channel, the chip offers different operating modes, briefly described hereafter.

Time-over-Threshold (ToT). . In this mode, the leading and trailing edge of the discriminator are captured by the TDCs. The charge is thus inferred from the measured pulse duration. The ToT readout allows to extend the charge sen-

sitivity beyond the saturation point of the front-end amplifier (50 fC nominal). In principle, either discriminator can be chosen, even though the one following the fast shapers provides more accurate timing information and it is thus the default choice in this mode.

Peak sampling. the output of the discriminator connected to the fast shaper is fed to the control logic, which generates a sampling pulse with a delay suitable to capture the slow shaper output around its maximum. The delay between the trigger given by the discriminator and the sampling pulse generated by the logic can be fine-tuned in steps equal to four clock cycles. For a 10 bit resolution, the maximum digitization time at 200 MHz clock is 5.12 μs, which allows an event rate of at least 200 kHz per channel in this modality.

Dual-threshold. mode. A lower threshold is set for the fast branch, thus allowing for time-walk minimization. The event is promptly discarded if the discriminator connected to the slow shaper, which has better signal-to-noise-ratio, does not fire within a predetermined time window.

3. ASIC performance

Fig. 3 shows the chip wire-bonded to the test printed circuit board. An external analog circuit allows to inject signals of well known charge at the preamplifier input. In this way, it is also possible to calibrate the test pulse generator embedded in the chip. Furthermore, a digital external pulse can be fed directly to the TDC inputs. The ASIC is configured, controlled and readout through a commercial FPGA board. The tests presented in this paper were done at a clock frequency of 160 MHz, which is, for system reasons, the operating frequency that will be use in the CGEM detector. As a first step, the TDC performance has been extracted by feeding a digital pulse at the TDC inputs and scanning it in step of 20 ps. These measurements allow also to fully characterized the behavior of the back-end electronics, which works according to expectations. As an example of the TDC performance, Fig. 4 and 5 show the time resolution of

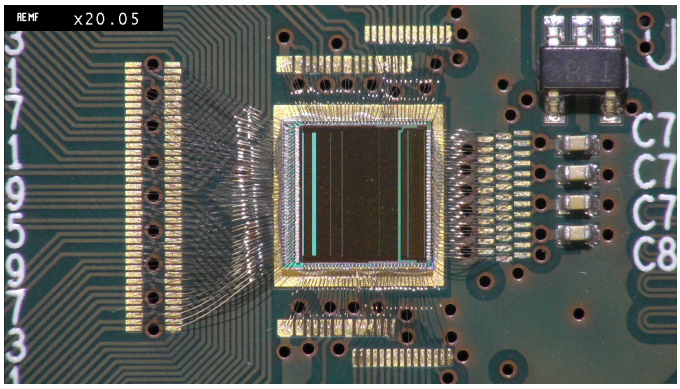

Figure 3: The TIGER ASIC wire-bonded on the test printed circuit board

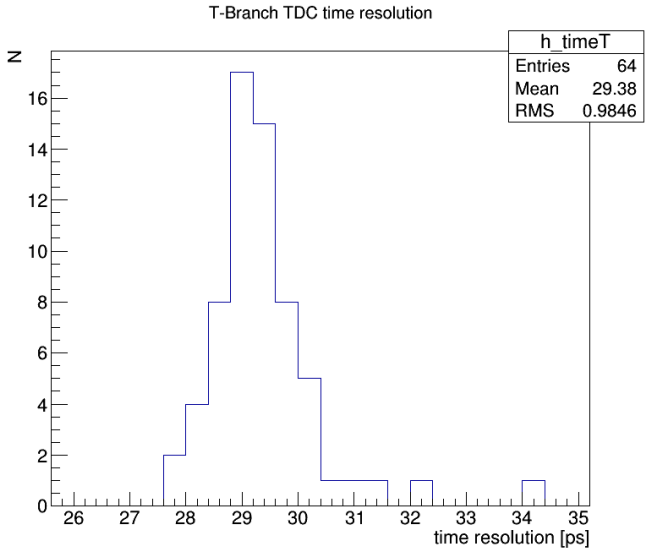

Figure 4: Time resolution of the TDC connected to the timing discriminator

the TDCs serving respectively to the timing and the energy discriminator. In both cases, an average rms quantization error of 30 ps is measured with good across-chip uniformity. Owing to the excellent behavior of the TDC, the system time resolution will be limited by the sensor and front-end amplifier characteristics. Since the sampling signal for the S&H is derived from the output of the comparator in the timing branch, it is important to to understand if the linear-

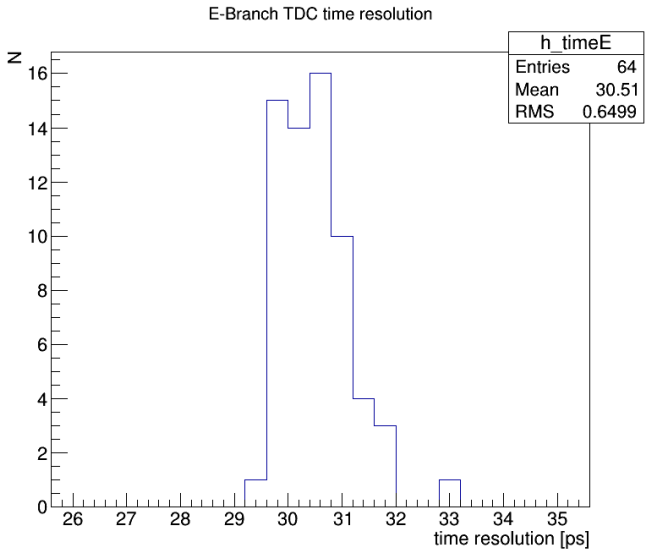

Figure 5: Time resolution of the TDC connected to the energy discriminator

ity of the circuit is affected by the discriminator time-walk. The test is done by injecting signals of different amplitudes with the external test pulse generator, which allows to explore the full dynamic range with enough granularity. The delay in the digital controller is chosen to put the sampling time in the region of maximum flat-top for the smallest signals. Fig. 6 shows the result of the linearity test. The plot reports the code of the internal ADC that digitzes the S&H output as a function of the input charge. The negative slope is due to the fact that the ADC works in reverse logic, hence smaller signal produce higher codes. The curve shows a good linearity of the circuit. This is confirmed by studying the deviation from linearity defined by the following formula:

$$NL = \frac{A_{th} - A_{meas}}{A_{th}} \tag{1}$$

where A_{th} and A_{meas} are respectively the theoretical expected value and A_{meas} is the experimental value, both expressed in ADC codes. The result is shown in Fig.7.

It must be pointed out that the measurement shows the non-linearity of the full chain, because the signal is injected at the input of the front-end amplifier.

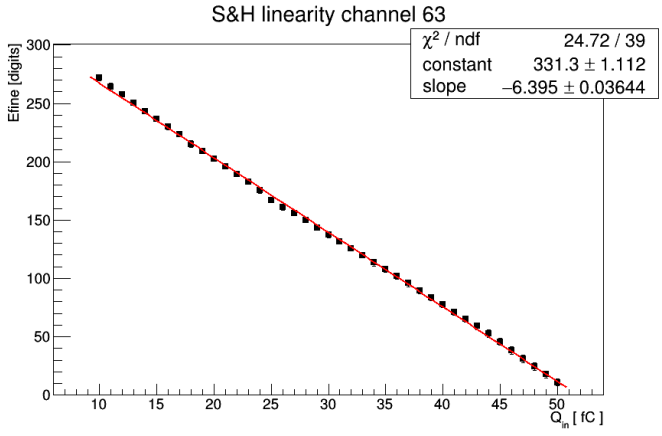

Figure 6: S&H ADC output code as a function of the input charge

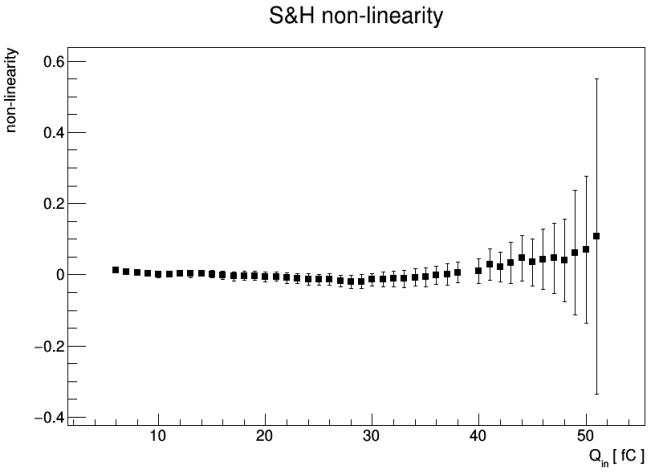

Figure 7: Front-end nonlinearity

The linearity is excellent (less than 0.2%) for most of the dynamic range, while a large degradation starts to be observed above 40 fC. On the basis of computer simulation, it is expected that the largest contribution to the non-linearity comes from a distortion in the shaper output stage. Test signals can also be fed to the amplifier input by the test pulse generator integrated on chip, which allows to selectively address all the channels in the ASIC. The resulting plot is shown in Fig.8. It can be seen from the figure that the gain measured with the internal

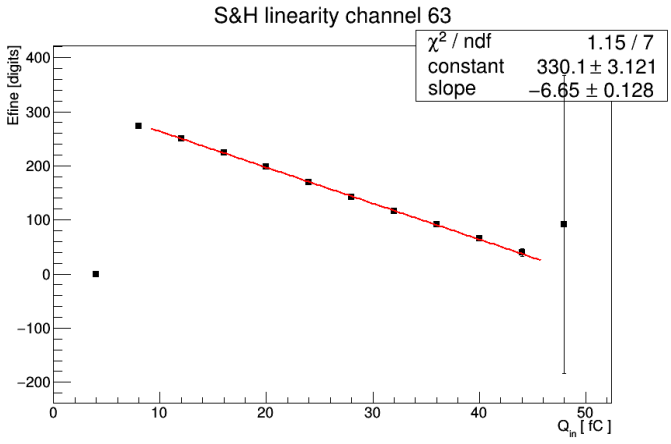

Figure 8: Linearity plot obtained with the test pulse generator integrated on board of the ASIC

circuit is compatible with that obtained with the external signal source in the middle-range, while the on-board pulser does not work properly at the edges of the dynamic range. This is attributed to the fact that signal amplitude is defined by regulating a current and for very small or very high values of this current some of the transistors in the pulse generator work outside the saturation region. While this point can be easily fixed in a next release of the ASIC by properly re-sizing the critical devices, the circuit is already good enough to assess the basic functionality of the individual channels.

The performance of the very front-end can also be assessed performing S-curve measurements Fig. 9 displays the gain of all 64 channels on one ASIC, measured through this method. In the test, an input signal of 8 fC is injected. An average gain of 10.76 mV/fC is found, which is very close to the 11 mV/fC expected from post-layout simulations.The rms gain variation is 3.1 mV on a 86 mV signal, which corresponds to a 3.5% rms dispersion. Due to the excellent linearity, the gain can be easily calibrated and off-line correction can be applied if needed. The S-curve measurement is also employed to extract the noise. Fig. 10 shows the input-referred noise expressed in terms of Equivalent Noise Charge (E.N.C.) as a function of the detector capacitance. The slope of

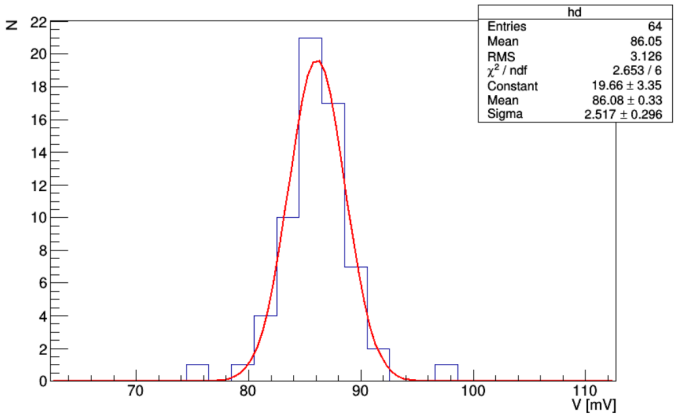

Figure 9: Gain distribution of all channels on one ASIC

10 e^-/pF matches well the one expected form computer simulations. A noise floor of 1500 e^- at zero detector capacitance is found. Finally, Fig. 11 reports

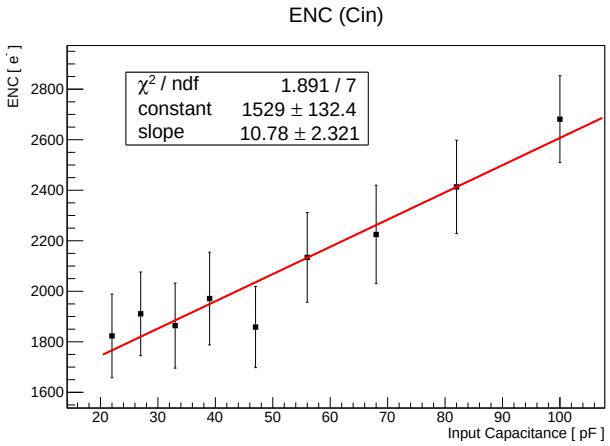

Figure 10: ENC versus input capacitance.

an example of charge measurement exploiting the Time-over-Threshold (ToT) principle. The non-linearity observed is due to the intrinsic pulse shape of $CR - RC^n$-like shapers. In this particular measurement only the coarse time information provided by the TDC is used. The measured ASIC performance are summarized in table 2.

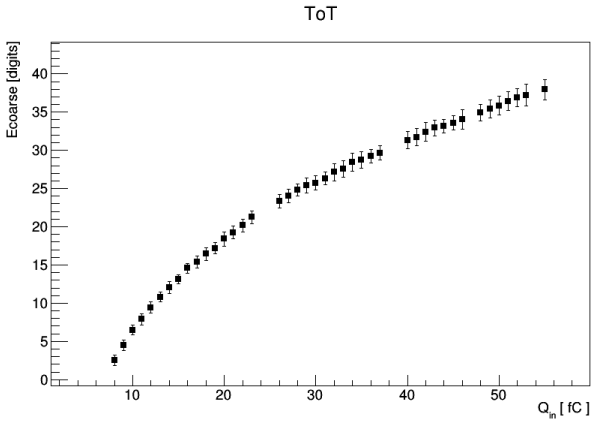

Figure 11: Example of charge measurement exploiting Time-over-Threshold (ToT).

Parameters	values
Input Charge	1-55 fC
TDC resolution	30 ps rms
Average gain	10.75 mV/fC
Nonlinearity: 1-40 fC	0.2%
Nonlinearity: 1-55 fC	1%
Rms gain dispersion	3.5%
Noise floors (ENC)	1500 e^-
Noise slope	10 e^-/pF
Maximum power consumption	12 mW/ch

Table 2: Measured performance of the TIGER ASIC

4. Conclusions

The ASIC presented in this paper has been designed to to read out the signals from the CGEM detector in the BESIII experiment. The chip is suitable for sensors with a total capacitance of up to 150 pF. Each of the 64 channels feature a low noise input and generates a time stamp with on-chip low-power TDCs. Charge measurement can be performed by peak detection or by Time-

over-Threshold. In peak detection mode the chip is linear in the $1 \div 50$ fC range. A detailed electrical characterization has been performed and the chip has been found functional at the first iteration on silicon. A noise floor of 1500 e^- rms and a noise slope of 10 e^-/pF have been measured. Due to the versatility of the back-end, new ASICs tightly optimised to a particular sensor can be derived in a relatively short time by redesigning only the very front-end. The final version of the chip has now been produced in a dedicated engineering run.

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