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A 64-channel ASIC for full waveform sampling with 200 MS/s for space-based cosmic-particles applications(*)

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Summary. — This paper discusses the development of a 64-channel Application-Specific Integrated Circuit designed in a commercial 65 nm CMOS technology to readout a camera plane composed of Silicon Photo-Multipliers. The purpose of the readout chain is the observation of Extensive Air Showers by detecting the Cherenkov radiation which signal is produced by Ultra-High Energy Cosmic Rays and Cosmic Neutrinos. Each ASIC generates a hitmap sent to an FPGA to analyze the pixel proximity. The stored data can be digitally converted on-chip if it is validated through this external checker. A single ASIC is formed by channels where 256 cells are connected to the output of the front-end electronics to obtain a full waveform sampling. An analog memory, a 12-bits Wilkinson Analog-to-Digital Converter and latches are placed into the cell unit working at 200 MHz clock. To derandomize the input signal, the array of cells is partitioned into segments of 32 cells each. The readout is realized using a serializer operating at 400 MHz in Double Data Rate. The ASIC is developed in the framework of the Extreme Universe Space Observatory - Super Pressure Balloon 2 mission, but it is also suitable for several other applications due to its configurability such as the partitioning and the resolution in the range of 8-12 bits. In this way, the chip can save power and conversion time, depending on the requirements of the experiment.

1. – Introduction

Ultra-High Energy Cosmic Rays (UHECRs) and tau leptons produced in the crust by Ultra-High Energy tau Neutrinos (UHENUs) generate Extensive Air Showers (EASs) during their passage through the terrestrial atmosphere. These cascades are made of relativistic particles which emit Cherenkov light collimated with the direction of the EAS propagation itself. This light emission can be used to track back both the direction and the energy of the primary UHECR/UHENU. The EAS parameters can be investigated

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using a proper optical system integrated into a telescope equipped with a focal plane of Silicon Photo-Multipliers (SiPMs). Placed at sub-orbital height ($\sim$ 30-40 km) or Low Earth Orbit ($\sim$ 500 km) the signal lasts typically tens of nanoseconds. As consequence of this evaluation a time resolution of the order of 100 MHz is mandatory to adequately process such kind of signals. Moreover a full waveform sampling approach lets to discriminate the EAS-related event from others such as those due to direct cosmic ray interaction. Because of these requirements, an Application-Specific Integrated Circuit (ASIC) called Multi-channel Integrated Zone-sampling Analogue-memory based Readout (MIZAR) was designed in a commercial 65 nm CMOS technology. Its implementation is inspired by current and next missions in the field of UHECR/UHENU observations such as Extreme Universe Space Observatory-Super Pressure Balloon2 (EUSO-SPB2) [1] flew on May 13^{th} 2023 on board stratospheric balloon platform and the next planned mission PBR (POEMMA Balloon with Radio) still under design, as well as Terzina [2, 3] and POEMMA [4] space-based missions.

In this context MIZAR was developed to carry out a complete acquisition chain, starting from the signal processing of the SiPMs to the digital conversion and the readout stage.

2. – MIZAR description

2˙1. *Camera architecture.* – Figure 1(a) illustrates a bare representation of a possible camera organized to accomodate SiPM tiles in its upper part and a board dedicated to the ASICs in the lower one. The signal transmission between the two boards is realized through an high-speed high-density socket here shown as blue place holders. The Input/Output (I/O) connections towards the Field Programmable Gate Array (FPGA) is made using a bank of shielded twisted pairs to communicate with the Low-Voltage Differential Signaling (LVDS) standard which is indicated as orange blocks. Each ASIC exploits 12 differential pairs to receive configuration and commands from the FPGA and to send data off-chip. Figure 1(b) depicts a more detailed layout of the board developed to collect the signals coming from 10 SiPM tiles. The red square is used as marker to point out the orientation of the SiPM and the connectors compared to the board.

2˙2. *ASIC architecture.* – Figure 2 represents a block diagram of the ASIC on multiple levels of hierarchy whose concepts have been previously explored in [5]. The leftmost part of the picture shows the general segmentation of the chip. The main digital logic

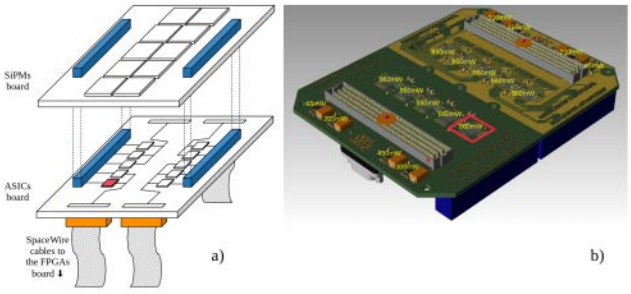

Fig. 1. – (a) A SiPMs board interfaced with the ASICs one in a tower-like structure. (b) The ASIC board with a preliminary power estimation of its main components.

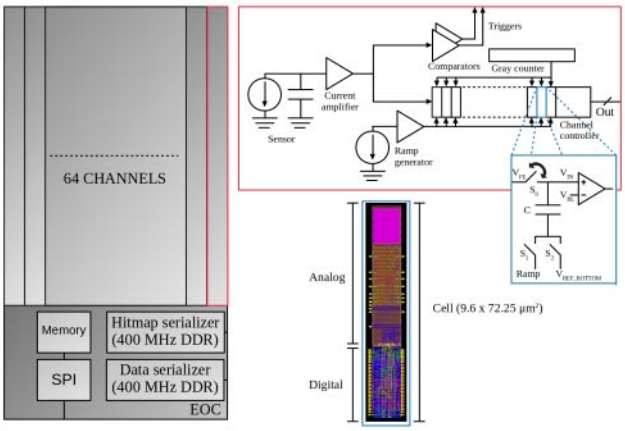

Fig. 2. – Block diagram representation of a channel, schematic of a cell and its layout.

has been implemented in the End-Of-Column (EOC) block where two serializers, a SPI module and the configuration registers are located. EOC manages the ASIC configuration and a group of Finite State Machines (FSM) implemented to carry out the sampling, the conversion and the readout of the data. These stages are realized through 64 channels whose schematic is illustrated in the rightmost-top part of fig. 2. Once a photon signal is detected by the sensor during the sampling, the SiPM induces a current signal processed by an amplifier. The output of this initial stage is then distributed between two comparators and an array of 256 cells. The first branch provides a local trigger pairs whose information is merged into the FSMs of EOC. When an event is detected through an internal priority scheme, the ASIC generates a hitmap and a flag rises up. If the event is accepted by the FPGA, the hitmap transmission is enabled. Then, the firmware performs a more detailed analysis to recognize interesting patterns. Thus, if the event is confirmed, the on-board digitalization takes place, followed by the readout stage, otherwise the system comes back to the sampling. These tasks are achieved distributing the sensor signal on the second branch connected to the cells. Latters are configurable into segments of 32 units each one named section. A single partition is able to independently perform an entire acquisition cycle and a channel can operate with segmentation of 32, 64 or 256 cells. This derandomized approach to the signal processing is an architectural choice to handle the Poissonian distribution of the events. Indeed in this way all the tasks can be achieved in parallel strongly reducing the dead times. Lastly, the righmost blue box of fig. 2 depicts the circuital schematic of the analog electronics embedded into a cell. Latter is equipped with a capacitor (C) and a comparator which form the core of a Wilkinson Analog-to-Digital Converter (ADC). The capacitor is exploited as analog memory of the sensor signal collected in the sampling stage closing both S_0 and S_2 switches and a pointer is used to enable S_0 cell by cell. During the digitization S_0 is opened, while C is disconnected from the voltage reference (V_{REF_BOTTOM}) and its bottom plate is connected to a ramp generator (RG) through S_1. The conversion enables both RG and a Gray counter working with the same phase. Thus, if the output of RG is increased by the Least Significant Bit (LSB) value, the Gray counter is incremented by one. When the voltage input V_{IN} is larger than voltage threshold V_{BL} the current value of the Gray counter is locally stored in the cell. The resolution is configurable in

a range between 8 bits and 12 bits, providing a key feature to the ASIC for such kind of application where an high granularity is not mandatory. Thus, the dead time due to the digitization process depends on the selected configuration and it can be considerably reduced. Since this time is equal to $2^N T_{clk}$ where N is the resolution expressed in number of bits and T_{clk} is equal to 5 ns because of 200 MHz clock, the conversion stage is included in a time window between $\sim 1.28\ \mu s$ and $\sim 20.5\ \mu s$ for 8 and 12 bits, respectively. The bottom part of fig. 2 represents the layout of a cell unit segmented into the analog circuitry and the digital logic. The total area of the cell is equal to 9.6 x 72.25 μm^2. Finally, the last stage is the data transmission performed with a dedicated serializer working in Double Data Rate (DDR) at 400 MHz. The stream is identified with an initial header (8 bits), followed by information about the packet (6 bits), a timestamp (16 bits), the address of the event (9 bits) and the data. Because of the configurable parameters, the length depends on the partition and the resolution selected. For instance, in the case of a 32-cells partition and a full-resolution of 12 bits, each channel will generate a data stream of 440 bits. Since the number of channels is 64, the serialization of this information at 400 MHz speed in DDR will require slightly more than $35\mu s$.

3. – Conclusions

This work described the implementation of a 64-channel ASIC for SiPMs readout realized in a commercial 65 nm CMOS technology. The chip is designed to provide an initial raw data representation to a FPGA through the generation of a hitmap. The SiPM signals are derandomized adopting a configurable channel partition and a programmable resolution in the interval 8-12 bits providing a flexibility to different application. The converted data is sent off-chip with a serializer working at 400 MHz in DDR.

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