Performance portability via C++ PSTL, SYCL, OpenMP, and HIP: the Gaia AVU-GSR case study

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Abstract—**Applications that analyze data from modern scientific experiments will soon require a computing capacity of ExaFLOPs. The current trend to achieve such performance is to employ GPU-accelerated supercomputers and design applications to exploit this hardware optimally. Since each supercomputer is typically a one-off project, the necessity of having computational languages portable across diverse CPU and GPU architectures without performance losses is increasingly compelling. Here, we study the performance portability of the LSQR algorithm as found in the AVU-GSR code of the ESA Gaia mission. This code computes the astrometric parameters of the $\sim 10^8$ stars in our Galaxy. The LSQR algorithm is widely used across a broad range of HPC applications, elevating the study's relevance beyond the astrophysical domain. We developed different GPU-accelerated ports based on CUDA, C++ PSTL, SYCL, OpenMP, and HIP. We carefully verified the correctness of each port and tuned them to five different GPU-accelerated platforms from NVIDIA and AMD to evaluate the performance portability (Ⴔ) in terms of the harmonic mean of the application's performance efficiency across the tested hardware. HIP was demonstrated to be the most portable solution with a 0.94 average Ⴔ across the tested problem sizes, closely followed by SYCL coupled with AdaptiveCpp (ACPP) with 0.93. If we only consider NVIDIA platforms, CUDA would be the winner with 0.97. The tuning-oblivious C++ PSTL achieves 0.62 when coupled with vendor-specific compilers.**

Index Terms—**High-Performance Computing, Performance portability, Portable languages, GPU programming, CPU and GPU architectures, Astrometry**

I. Introduction

The scientific data produced by experiments in different domains are quickly increasing in size, approaching the $\sim$10-100 PB range. Processing such amounts of data in a reasonable time requires Peta- and Exa- FLOP/s of computing capacity. Today such compute capacities are achieved using accelerated supercomputers comprising O(10^3) computational nodes having one or more accelerators, such as GPUs. The inclusion of GPU accelerators adds a new dimension of heterogeneity that further exacerbates the long-standing problem of code and performance portability across successive generations of supercomputers typical of the HPC domain. Indeed, the top supercomputers are often one-off projects with HPC applications relying on end-to-end hardware/software co-design using low-level code to achieve extreme compute scalability and efficiency. Co-design intercepts thriving trends, such as hardware functional specialization, the need for power capping, and the expanding HPC application space. Still, it requires suitable abstractions to avoid the explosion of time-to-solution, which is utterly needed by the growing community of industrial supercomputing users.

An alternative method is re-adapting the application structure to fully exploit GPU-accelerated compute node capabilities. While it might not be as effective as co-design for achieving record performance, it can improve the scalability of legacy parallel codes. Code adaptation also aims to express some of the application's functional steps as algorithmic patterns that map well into available hardware features. This kind of code porting and tuning is typical, e.g., with CUDA [1] and HIP [2], the respective low-level native programming languages for NVIDIA and AMD GPUs that allow programmers to access GPU-specific hardware features, such as scratchpad memory and tensor cores. As for any vendor-specific low-level language, the optimized code is confined to run on specific hardware platforms and might require re-tuning on different boards, even from the same vendor.

Both end-to-end co-design and vendor-specific low-level languages are useful for producing record-breaking applications. Still, they face sustainability and cost limitations for many applications of significant industrial interest. Indeed, for industrial users, the ability to preserve investment in code development and tuning across different generations of platforms significantly affects their entire value chain linked to supercomputers. The advent of GPU-accelerated supercomputers makes this need evermore compelling.

To address code portability several programming frameworks that aim to decouple the application from specific hardware platforms with no (or limited) performance loss, have been recently proposed. Examples are C++ Parallel Standard Template Library (PSTL) [3], HIP [2], KOKKOS [4], OpenMP with GPU offload [5], OpenACC [6], RAJA [7], OCCA [8], SYCL [9], Alpaka [10] and Fastflow [11]. The use of such models raises the concept of *performance portability*, which is becoming a crucial research point in HPC [12]. While this term has undergone various definitions [4], [13], [14], at large, it aims to capture "an application's performance efficiency for a given problem that can be executed correctly on all platforms in a given set" [15].

Differently from related work studying the performance portability of specific tasks (e.g., [16]) or synthetic benchmarks (e.g., [17]), our study dwells into the performance characteristics of a scientifically and computationally relevant real-world application: the Astrometric Verification Unit-Global Sphere Reconstruction (AVU-GSR) pipeline of the European Space Agency's (ESA) Gaia mission. This pipeline aims to find the astrometric parameters of $\sim 10^8$ primary stars [18] in the Milky Way with a 10-100 micro-arcseconds accuracy [19]. At the core, this requires solving a system of linear equations done via a Solver module which implements a customized and parallelized version of the iterative LSQR algorithm [20], [21] to be able to deal with the problem specific structure of the data. This code has been uses in production since 2014 at the CINECA supercomputing center. The LSQR solver is the crucial computational unit in the pipeline and the object of your analysis. For sake of simplicity, hereon we use the term "AVU-GSR" for the LSQR solver of the pipeline alone.

Malenza et al. [22] studied the weak scalability of two ports of the AVU-GSR code, written in CUDA [23], and C++ PSTL, on up to 256 nodes of Leonardo[1] with NVIDIA A100 GPUs. Here, we add further programming frameworks, notably HIP, OpenMP with GPU offload (OpenMP-GPU), and SYCL, verify their correctness, and study their performance portability using Pennycoock's Φ score across five different compute architectures from both NVIDIA and AMD.

Our main contributions can be summarized as follows:

- We study the parallelization of ESA's AVU-GSR solver and port it to HIP, OpenMP-GPU, and SYCL. The choice stems from the promising results and properties described in literature [2], [3], [5], [9].
- We validated the correctness of each port using reference datasets from production and tune each port for optimal performance obtaining a speedup of up to $\sim$ 2x over the CUDA version currently used in production.
- We experimentally determine the Φ performance portability score of eight programming frameworks and compiler combinations across five hardware platforms, four based on NVIDIA, and one based on AMD, using three problem sizes.

Paper roadmap. In §II, we present literature works related to our analysis. In §III, we illustrate the main scientific motivation of our study and the structure of the Gaia AVU-GSR code. In §IV, we describe the parallelization and optimization strategies of the code version. In §V, we present our results in terms of performance portability and code validation. §VI concludes the paper and presents future works.

II. Background and Related works

Performance portability metric. Performance portability aims to capture two critical aspects: the capability of applications to run across a designated set of heterogeneous hardware platforms and the achieved performance. Various metrics have been used [4], [13], [14]. While a universally accepted metric is still lacking, Φ introduced by Pennycook et al. [15] has rapidly gained traction. Φ is defined as follows:

$$\Phi(a,p,H) = \begin{cases} \frac{|H|}{\sum_{i \in H} \frac{1}{e_i(a,p)}} & \text{if } i \text{ is supported } \forall i \in H \\ 0 & \text{otherwise,} \end{cases} \tag{1}$$

where a is a specific application, p is a given problem that the specific application a computes and $e_i(a,p)$ is the efficiency of the application a for the problem p on a platform i from a given set of H of size $|H|$. In other words, Φ is the harmonic mean of the application's efficiency over the set of platforms H. As such, if the Φ of a specific application across a set of platforms is lower than the Φ across a different set of platforms, it does not necessarily mean that this application has worse performance on the first set of platforms compared to the second one. Φ measures the imbalance of platform support across different code versions, not their absolute efficiency. If an application is not able to run on all platforms in H, the Φ is 0 by definition.

Performance portability studies. Several studies address performance portability. Pennycook et al. [15] describe some real-life examples of the usage of the Φ metric. They present the GPU-STREAM benchmark [24], a reimplementation of McCalpin's STREAM benchmark [25], parallelized with eight programming models (McCalpin, SYCL, RAJA, KOKKOS, OpenMP-C++, OpenACC, CUDA, and OpenCL) and evaluated on 12 different platforms, either CPU or GPU-based. Since none of the benchmarks is able to run on all platforms, the Φ is calculated for different sets of code versions and platforms.

Lin et al. [26] test the performance portability of three heterogeneous high-performance computing (HPC) mini-applications (BabelStream, miniBUDE, and CloverLeaf) on both CPU and GPU platforms using different implementations of the C++17 PSTL. The three mini-applications cover both compute-bound and memory bandwidth-bound cases. The authors prove the ports to be competitive with previous versions written in OpenMP, CUDA, SYCL, and Kokkos across different platforms, but they avoid evaluating the performance portability of these mini-applications with an objective metric. Bhattacharya et al. [27] investigate different portable parallel programming models (KOKKOS, SYCL, OpenMP, C++ STL) for high energy physics use cases (FastCaloSim, ACTS, Wire Cell, Patatrack, P2R, and Random Number Generators) highlighting their benefits and challenges. Atif et al. [28] added the Alpaka parallelization language to the previous study. Other works study performance portability from the perspective of the (pre-)Exascale era. Some of them are [29]–[31]. Such studies only address benchmarks or mini-apps or lack the use of a wider-spread metric. Differently from them, we use a real-world application using the recognized Φ metric.

III. Gaia Mission and AVU-GSR Code

A. Scientific relevance of the Gaia mission

The Gaia mission was launched on December 19th 2013, and it is expected to end its life at the beginning of 2025,

[1]https://www.hpc.cineca.it/systems/hardware/leonardo/

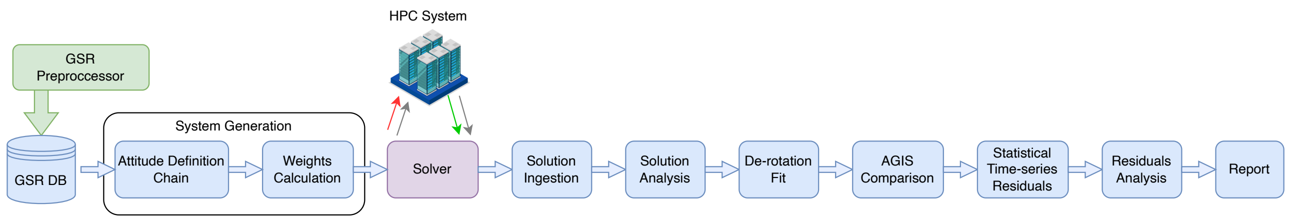


Fig. 1: Description of the pipeline of the AVU-GSR mission code. The solver (in purple) is the main computation bottleneck offloaded to an HPC system.

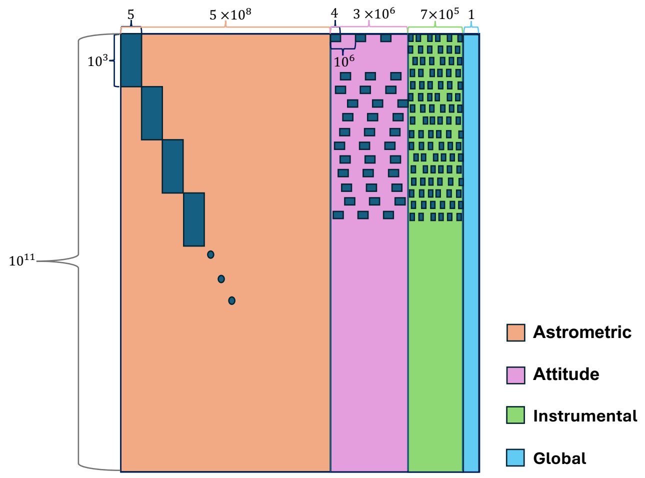


Fig. 2: Structure of matrix $\mathbf{A}$. Non-zero parameters are highlighted as dark blue blocks.

after about seven-years extension from its initial planned end (2018)[2]. This is due to the relevant scientific worth provided by the mission. Gaia mission is producing an extremely accurate astrometric map of more than 10^9 stars in the Milky Way, measuring their parallaxes, right ascension, declination, and proper motions, besides their luminosity, temperature, and composition [32]. The accuracy of the astrometric measurements can go down to the 10-100 micro-arcseconds level or below [32]. High-resolution astrometry is a powerful instrument for exploring essential questions related to our Galaxy's origin, structure, and evolutionary history. High-resolution astrometry, in synergy with high-resolution spectroscopy and photometry, allows to build extremely precise kinematic profiles of our Galaxy (rotation curves and vertical velocity dispersions) [33], [34] and to study the formation and evolution of the Milky Way (e.g., [35]–[37]). Moreover, it can shed light on disentangling between General Relativity, the current most explored theory of gravity which assumes that galaxies are surrounded by large dark matter halos, and other theories of modified gravity, which do not resort to dark matter (e.g., [34], [38]–[42]).

B. The Gaia AVU-GSR code

The Gaia AVU-GSR code determines the astrometric parameters of the primary stars in the Milky Way ($\sim10^8$ stars), as well as the attitude and instrumental specifications of the Gaia satellite and the global parameter γ of the Parametrized Post-Newtonian (PPN) formalism, with a high precision around $10-100$ micro-arcseconds. To find these parameters, the Gaia AVU-GSR code solves an overdetermined system of linear equations [19], [22], [23], [43]–[46], choosing between two fully-relativistic astrometric models [47], [48]:

$$\mathbf{A} \times \vec{x} = \vec{b}, \tag{2}$$

where $\mathbf{A}$ is a large coefficient matrix with a high degree of sparsity, $\vec{b}$ is the vector of known terms and $\vec{x}$ is the array of unknowns. The number of rows of $\mathbf{A}$ represents the number of equations which is equal to the number of stars times the number of observations per star, i.e., $\mathrm{O}(10^{8+3})$. The number of columns of $\mathbf{A}$ represents the number of unknowns dominated by the 5 astrometric parameters per star, i.e., $\mathrm{O}(10^8)$. Fig. 2 depicts the structure of the matrix. The matrix is highly sparse with a block diagonal structure for the astrometric parameters, whereas the structure of the attitude parameters depends on a stride stemming from the measurement campaign, and the instrumental part has an irregular pattern. The global part has, at maximum, one parameter per row, different from zero. Saving only the nonzero elements of $\mathbf{A}$ allows to reduce the problem by seven orders of magnitude. The obtained reduced matrix, $\mathbf{A}_\mathrm{r}$, has the same number of rows as $\mathbf{A}$ and contains at most $\sim (10^{11}) \times 24$ elements, i.e., 5 astrometric, 12 attitude, 6 instrumental, and 1 global parameters per row. The dark blue blocks in Fig. 2 (not in scale) illustrate how the non-zero parameters distribute in each row of the astrometric, attitude and instrumental parts.

To store the matrix in memory, we leverage the inherent properties of the matrix. Specifically, we split A_r into four submatrices (one for the astrometric, attitude, instrumental, and global parameters) differently treated according to their structure. The astrometric submatrix is structured with a block diagonal pattern, with each block row only containing five contiguous non-zero elements (Figure 2). To efficiently store this system, we only need to save the starting column index of the astrometric non-zero elements for each row of $\mathbf{A}$ in an

[2]https://www.esa.int/Science_Exploration/Space_Science/Gaia

array called `matrixIndexAstro`. For the attitude parameters system, each row of $\mathbf{A}$ contains 12 non-zero elements arranged in three blocks of four elements each, with a defined stride (Figure 2). Knowing this pattern allows us to only store the index of the first attitude non-zero element in each row of $\mathbf{A}$ in an array named `matrixIndexAtt`. Unlike the other submatrices, the instrumental parameters lack a predictable pattern (Figure 2). As a result, we store, for each row of $\mathbf{A}$, the column indexes of all instrumental non-zero elements in an array called `instrCol`. Overall, the astrometric submatrix represents $\sim$90% of the memory footprint while the other parts (attitude, instrumental, and global) the remaining $\sim$10%. Overall, $\mathbf{A}_{\mathrm{r}}$, $\vec{b}$ and $\vec{x}$ occupy $\sim$19 TB, $\sim$800 GB and $\sim$4 GB, respectively.

The system solution is iteratively obtained through a customized and preconditioned version of the LSQR algorithm [20], [21], which approximately takes the $\sim$95% of the AVU-GSR solver. The algorithm stops when it reaches convergence or the maximum number of iterations. The most intensive computation of the single LSQR iteration is the execution of the *aprod1*,

$$\vec{b}^i + = \mathbf{A} \times \vec{x}^{i-1}, \tag{3}$$

and *aprod2*,

$$\vec{x}^i + = \mathbf{A}^T \times \vec{b}^i, \tag{4}$$

functions. In (2), the number of equations is larger than the number of unknowns, which makes the system overdetermined. Therefore, some constraint equations must be set to derive a univocal solution.

IV. Parallelization of the Gaia AVU-GSR Code

The Gaia AVU-GSR code leverages distributed systems via MPI, where each MPI rank processes a subset of the observations. To fully exploit the compute accelerators, the code is further parallelized by offloading the main arithmetic computations on GPUs using CUDA [23], [46]. In particular, the two most intensive computations are implemented as four kernels (one for each submatrix) respectively named as *aprod{1,2}_Kernel_astro()*, *aprod{1,2}_Kernel_att()*, *aprod{1,2}_Kernel_instr()* and *aprod{1,2}_Kernel_glob()*.

Kernel parallelization. The *aprod 1* kernels result in rows of matrix times column vector multiplications, which can be easily parallelized. Instead, due to the irregular structure of transposed $\mathbf{A}$, the indexes used by *aprod2* can collide (with the exception of the astrometric parameters due to their block diagonal structure), and hence the updates require atomic operations. To minimize the collision probability, we redesigned the code to reduce the number of blocks and GPU threads per block in the regions where atomic operations are performed. However, this can imply that, in some cases, the GPU occupancy is not maximally exploited. To limit stalling times, we execute the kernels in streams, allowing their asynchronous overlap. Since the atomic operations in each submatrix target different subsections of $\vec{x}$, the asynchronous execution of the kernels does not increase the execution cost of the atomic operations.

Parallel programming frameworks. In addition to an optimized CUDA implementation leveraging the observations above, we parallelize the LSQR solver using four different additional parallel programming frameworks: HIP, SYCL, OpenMP, and C++ PSTL. CUDA, HIP and SYCL are language-specific, meaning they have explicit run-time functions that users can use to manage memory and write fine-tuned kernels [49]. OpenMP, similarly to OpenACC, is a directive-based API [50]; this means the user can add `pragma` directives that instruct the compiler to generate assembly code that runs on multicores systems and, eventually, accelerators. Generally, pragma-based programming languages are easier to use compared to language-specific frameworks as users are not required to re-write the entire application, and do not require explicit tuning and memory management to offload computation on GPUs or multicore systems. Another way to execute applications on GPUs is developing code with specific abstraction libraries that translate user code into CUDA, HIP or OpenMP code. Examples of such libraries are KOKKOS, RAJA, Alpaka, Thrust, and C++ PSTL. Here, we used the C++ PSTL as it is an open standard that only requires the standard library, completely masking any low-level parallel runtime library. Starting from C++17, standard algorithms can be executed in parallel specifying the execution policy [51]. Offloading computations to GPU requires implicit memory mapping mechanics between host and device and a back-end that is able to generate GPU assembly code.

a) The CUDA code: The CUDA version allocates the host variables via *cudaHostMalloc* to use pinned memory. All variables needed by the GPU are allocated using *cudaMalloc*. The four submatrices are copied asynchronously to GPUs, using *cudaMemcpyAsync*. The same is done with all relevant quantities, constraints, and other unknowns of the astrometric problem. CUDA streams are used to overlap *aprod2* kernel computations. It is worth noting that the matrices are copied to the GPU before the main loop and remain there until the end of the algorithm, avoiding costly GPU-CPU data exchanges during loop iterations. We force the same behavior on all frameworks, allowing explicit memory management.

b) Porting from CUDA to HIP: Since HIP is a programming language designed to be syntactically similar to CUDA, porting was relatively easy. Initially, we used HIPIFY to translate our code into HIP, and then we optimized the code, tuning kernel parameters for AMD and NVIDIA architectures. In particular, *cudaMalloc*, *cudaMemcpyAsync*, and *cudaStreamCreate* were replaced with *hipMalloc*, *hipMemcpyAsync* and *hipStreamCreate*. One thing worth noting is that, same as with C++ PSTL, we allocate the memory using *hipMemAdvise* and forcing coarse grain. This is done for performance reasons as we observed experimentally that fine-grain coherence led to performance degradations due to the atomic operations contained in the *aprod2* kernels.

c) Porting from CUDA to SYCL: The SYCL implementation uses order queues and Unified Shared Memory allocators.

TABLE I: Software Versions on NVIDIA architectures

	T4 & V100	A100	H100
CUDA	12.3	11.8	12.3
NVC++	24.3	24.3	24.3
AdaptiveCpp	24.06	24.06	24.06
HIP	5.7.3	5.7.3	5.7.3
Clang	17.0.6	17.0.6	17.0.6
DPC++	19.0.0	19.0.0	19.0.0

In particular, `malloc_device` allocates data directly on GPU. We used `parallel_for` to declare parallel code regions and `NDrange` to fine-tune kernels.

d) Porting from CUDA to OpenMP: We used the OpenMP `#pragma omp enter data` directive to allocate GPU data and the OpenMP `#pragma omp target update` directive to update it. Data are processed on GPU using `#pragma omp target teams distribute parallel for`. Kernels can be fine-tuned by setting the number of teams `num_teams` and the thread limit `thread_limit`.

e) Porting from CUDA to C++ PSTL: The first porting of the code to C++ PSTL was done in [22]. It is worth noting that, in this case, there is no specific directive to tune the number of threads and blocks to be used by the kernels.

V. Results

A. Software stack and hardware platforms

We measured the Ψ metric considering only runs using a single GPU. We used the following hardware platforms:

- **GraceHopper**: CPU: 1x NVIDIA Grace CPU (72 Arm Neoverse V2 Cores @ 3.0 GHz); GPU 1x NVIDIA HOPPER H100, 96 GB HBM3e; MEM: 574 GB LPDDR5X; Driver Version: 545.23.08; CUDA Version: 12.3;
- **EpiTo**: CPU: 1 Ampere Altra Q80-30 CPU (80-core Arm Neoverse M1); GPU: 2 x NVIDIA A100 GPU, 40 GB HBM2 each; Driver Version: 515.65.01; CUDA Version: 11.7;
- **CascadeLake**: CPU: 1 Intel(R) Xeon(R) Gold 6230 CPU; GPU: 1 x NVIDIA V100S GPU, 32 GB HBM2; 1 x NVIDIA T4 GPU, 15 GB GDDR6; Driver Version: 550.54.15 ; CUDA Version: 12.4;
- **Setonix**: CPU: 1x AMD EPYC 7742 (64 cores@2.25 GHz); GPU: 4x AMD MI250x, 512 GB HBM2; MEM: 512 GB DDR4;

Since we mainly target the performance using accelerators and each platform has a different GPU, hereon we identify each platform via the name of the equipped GPU. We compare the performances of the different implementations using the LSQR iteration time. Since the AVU-GSR code is based on an iterative algorithm, we believe that the iteration time is a good estimator of the application performance. We used code profilers from NVIDIA and AMD to verify that most of the time of this code is spent computing the matrix-by-vector products of *aprod1* and *aprod2*.

TABLE II: Compilation Flags on NVIDIA architecture

P. Frameworks	Compilation Flags
CUDA	`-gencode=arch=compute_XX,code=sm_XX`
HIP	`--gpu-architecture=sm_XX`
SYCL	
acpp	`--acpp-platform=cuda` `--acpp-targets=cuda:sm_XX` `--acpp-gpu-arch=sm_XX`
DPC++	`-fsycl -fsycl-targets=nvptx64-nvidia-cuda` `-Xsycl-target-backend` `--cuda-gpu-arch=sm_XX`
OpenMP	
clang++	`-fopenmp -fopenmp-targets=nvptx64-nvidia` `-cuda -Xopenmp-target=nvptx64-nvidia-cuda` `-march=sm_XX`
nvc++	`-mp=gpu -gpu=ccXX,sm_XX`
PSTL	
acpp	`--acpp-platform=cuda --acpp-stdpar` `--acpp-targets=cuda:sm_XX` `--acpp-stdpar-unconditional-offload` `--acpp-gpu-arch=sm_XX`
nvc++	`-stdpar=gpu -gpu=ccXX,sm_XX`

a) Software stack on NVIDIA architecture: We built the compilers from source for each platform using `gcc-12.2.0` as base compiler. Table I and Table II summarize the compilers and compiler flags used for each framework. CUDA and HIP versions were compiled with `nvcc` and `hipcc`. We compiled mostly all code with the flag `-std=c++20 -O3`. For CUDA and HIP versions on EpiTo we used `-std=c++17` for default system setting reasons. The same C++ standard version was used for the SYCL code when compiled with `DPC++` compiler.

b) Software stack on AMD architecture: On AMD, we used the `rocm-5.7.3` toolkit installed on the Setonix system to compile HIP and OpenMP code. OpenMP code was also compiled with native clang compiler version `17.0.6`. We installed the AdaptiveCpp compiler version `24.06` to compile SYCL and C++ PSTL versions. We installed `rocm-stdpar` compiler version `18.0.0` for C++ PSTL and `DPC++` compiler `18.0.0` for SYCL. Table III summarizes all compilation flags used. All codes were compiled using the additional `-std=c++20 -O3` flags.

B. Performance portability

We measure the Ψ of all code versions across the platforms listed in §V-A using the application efficiency based on the average iteration time of the solver. To ensure that our ports are representative of the application's best performance, we did a preliminary comparison of our optimized CUDA version against the production version of the code, obtaining a speed-up of 2.0x on Leonardo on a 42 GB problem.

The considered accelerators vary in their available device RAM capacity. Since the GPU memory occupancy is closely related to the size of the **A** matrix (copied only once before the main iteration cycle), we tested problems of different sizes close to the limit of the different GPUs, in particular: 10 GB (on all devices), 30 GB (all except Tesla T4) and 60 GB (only

TABLE III: Compilation Flags on AMD architecture

P. Frameworks	Compilation Flags
HIP	`--offload-arch=gfx90a -munsafe-fp-atomics`
SYCL	
acpp	`--acpp-platform=rocm --acpp-targets=generic --acpp-gpu-arch=gfx90a -munsafe-fp-atomics`
DPC++	`-fsycl -fsycl-targets=amdgcn-amd-amdhsa -Xsycl-target-backend --offload-arch=gfx90a`
OpenMP	
clang++	`-fopenmp -fopenmp-targets=x86_64, -fopenmp-targets=amdgcn-amd-amdhsa -Xopenmp-target=amdgcn-amd-amdhsa -march=gfx90a`
amdclang++	`-fopenmp --offload-arch=gfx90a -munsafe-fp-atomics`
PSTL	
acpp	`--acpp-platform=rocm --acpp-stdpar --acpp-targets=hip:gfx90a --acpp-stdpar-unconditional-offload --acpp-gpu-arch=gfx90a -munsafe-fp-atomics`
clang++	`--hipstdpar --hipstdpar-path=$(HIPSTDAR_ROOT) --offload-arch=gfx90a -munsafe-fp-atomics`

on H100 and MI250X)[3]. We report the average iteration time over 100 iterations, and repeat each experiment 3 times to enhance its statistical robustness.

Using the p3-analysis-library [52], we plot the application efficiency and Ⴔ for all platforms and frameworks for each problem size in Fig. 3. In each subfigure, the plot on the top left shows how efficiency varies across frameworks and platforms. Lines identify the AVU-GSR solver implemented using different framework-compiler pairs. In particular, the first value on the x-axis describes the maximum efficiency on the best-performing hardware for a given framework. The hardware platform itself is identified by the letter in the plot below on the row with the line of the same color. The right top plot shows instead the performance portability computed using Eq. (1) across all platforms. The green and violet lines illustrate the efficiency of OpenMP code when compiled with the base clang (OMP+LLVM) and the vendor compilers (OMP+V), respectively. The brown and gray lines depict the efficiency of C++ PSTL when using AdaptiveCpp (PSTL+ACPP) and vendor compilers (PSTL+V). Lastly, the yellow and cyan lines represent the efficiency of SYCL when compiled with AdaptiveCpp (SYCL+ACPP) and DPC++ (SYCL+DPCPP)[4].

To dive deeper into the results, we also report, in Fig. 4 and 5, the average iteration time and application efficiency of all frameworks on the different platforms. Each figure comprises three subfigures that show the results for the three problem sizes.

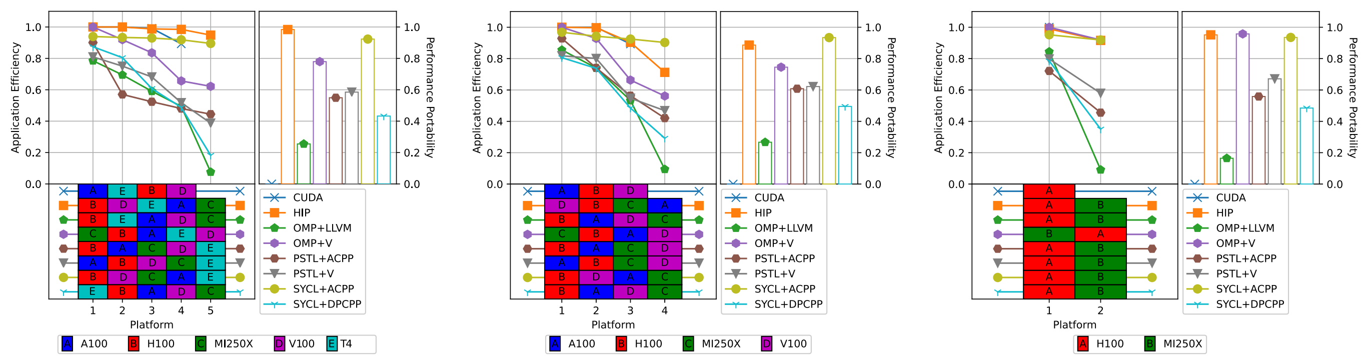
Fig. 3a, Fig. 3b and Fig. 3c show the results for a problem size of 10 GB, 30 GB, and 60 GB, respectively. For a 10 GB problem, the highest Ⴔ was achieved by HIP (0.98) followed by SYCL+ACPP (0.92). Apart from CUDA's Ⴔ value, which is zero by definition since it cannot be executed on AMD GPUs, the worst value is 0.25 obtained by OMP+LLVM, and all others lying somewhere in between. Interestingly, the best efficiency is obtained on the most recent NVIDIA hardware, i.e., H100, for 4 out of 8 frameworks, including even HIP. MI250X is, instead, the best platform for OMP+V. Surprisingly, T4 is the best platform for SYCL+DPCPP. Only V100 has never been the best platform for any of the frameworks. When considering the results on a bigger problem, i.e., 30 GB (shown in Fig. 3b), the overall application efficiencies vary more leading to generally lower performance portability scores. Here the best score is 0.93 by SYCL+ACPP which surpasses HIP with a score of 0.88. The framework with the worst drop in efficiency is OMP+LLVM which goes from 0.85 on H100 to 0.53 on V100. The best platform remains H100, which is the first choice for half the frameworks and the second best for the remaining half. Unsurprisingly, the MI250X is the best platform for HIP. Only two GPUs have enough memory to support the 60 GB problem: H100 and MI250X. The trends shown before are confirmed here too, but overall, more frameworks obtain high scores due to the low number of hardware platforms. Not considering the MI250X, CUDA would achieve a Ⴔ score of 0.97 and 0.96 for the 10 GB and 30 GB problem sizes, respectively. Note that there is no meaning to compute Ⴔ from the 60 GB problem since we have only one NVIDIA GPU supporting that size in our test platforms.

The figures clearly show that HIP and SYCL+ACPP (and CUDA when considering only NVIDIA GPUs) obtain the best Ⴔ scores stemming from high application efficiency scores. This is partially confirmed by the results shown in Figs. 4 and 5. While, as expected, newer and more performant platforms clearly deliver lower average iteration times across all model sizes, given a platform, the fastest time is typically given by CUDA (mostly on T4 and A100) or HIP (mostly on V100 and H100) frameworks. Surprisingly, the best framework on MI250X is OMP+V, however it is clearly outperformed on the NVIDIA-accelerated platforms by the other frameworks leading to a lower Ⴔ score (between 0.95 and 0.45 across the three problem sizes). Instead, SYCL+ACPP, while not being the best on any platform, achieves similar application efficiencies across all the tested hardware.

CUDA, HIP, and SYCL allow hand-tuning of the GPU kernels. Indeed, different numbers of blocks and threads of the kernels produce different performance results. In our experiments, we tuned the parameters of the CUDA, HIP, and SYCL kernels for each platform, achieving up to 40% reduction in iteration time. This testifies how relevant tuning such frameworks can be. Unfortunately, different platforms often require different tuning. The best SYCL performance is

[3]Bigger problems can be addressed using multiple GPUs eventually on multiple nodes which is out of scope of this paper.

[4]Hereon, for simplicity we refer to framework as specific framework plus compiler combinations



(a) 10 GB Problem (b) 30 GB Problem (c) 60 GB Problem

Fig. 3: Performance portability for problems of size: a) 10GB, b) 30GB, and c) 60GB.

obtained using the AdaptiveCpp compiler. SYCL code compiled with the DPC++ compiler offers lower performance. This can be due to incorrect compilation or suboptimal parameter tuning. We kept the same tuning configurations adopted for AdaptiveCpp.

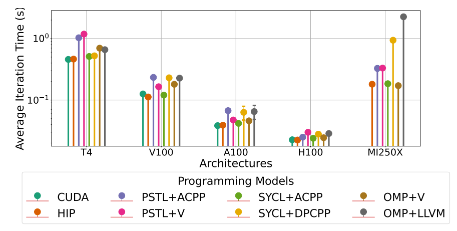
The other frameworks do not allow easy tuning of the GPU kernels. The default compiler tuning produced a code that, on H100, achieved 91% and 84% of the CUDA performance, when compiled with `nvc++` and standard `clang++`, respectively, approximately on all problem sizes. On other platforms, OpenMP performed slightly less but still between 83% and 59% of the best-achieved performance with comparable performance on both compilers.

The C++ PSTL efficiency increases from T4 to H100, reaching a value of 90% application efficiency on H100 coupled with ACPP and problem sizes of 10 GB and 30 GB. `nvc++` compiler performs slightly better than ACPP on H100 for the 60 GB problem size reaching 79%. As for OpenMP, both compilers achieve comparable performance, even if ACPP does not explicitly use the system unified shared memory mechanism [53] while it is required by `nvc++`. The increasing performance trend mirrors that of more performant hardware, so we hypothesize that it is due to the different technical characteristics of the considered GPUs. As said in §IV, with C++ PSTL we cannot explicitly set the kernels parameters yet. Using the `nsys` profiler, we saw that the default parameter tuning spans 256 threads per block on each architecture. While this number of threads efficiently optimizes the kernel's execution on H100 and A100, it is less efficient on the weaker T4 and V100, where, as seen from the kernel's tuning of the CUDA code, the number of threads that give best performance is 32. The C++26 proposal [54] aims to include executors in the STL. This feature will potentially allow to set explicit kernel parameters and, hence, reduce the observed performance gap among the platforms.

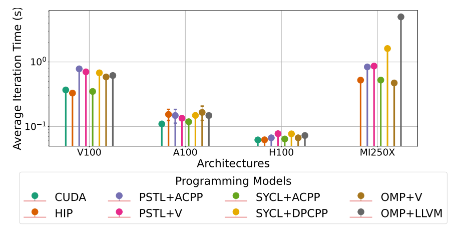
A special note goes to the performance on MI250X. Even with a powerful GPU the observed performance is slower than on the NVIDIA architectures, especially A100 and H100. This is mainly due to how the `aprod{1,2}` kernels were originally written. To verify this hypothesis, we take similar SpMV kernels, implemented using HIP by amd-lab-notes [55], and test them on matrix sizes similar to our own. We tested them on A100 and MI250X architectures. Indeed, the performance was similar to the one obtained by our AVU-GSR solver. We hypothesize that the lower performance is due to noncoalescent memory accesses by threads. We tried to maximize performance by kernel tuning and noted that low numbers of threads and blocks offer the best performance. OpenMP code compiled with `amdclang++` is the one that achieves the best performance on all considered problem sizes. We tuned the OpenMP kernels with parameters similar to the ones used by HIP and SYCL as the default compiler tuning brought lower performance. HIP and SYCL perform similarly to OpenMP when compiled with `hipcc` and `acpp`, respectively. While SYCL code compiled with `DPC++` compiler and OpenMP code compiled with base `clang++` compiler gives lower performance. This is due to the fact that some compilers could not generate code that uses atomic read-modify-write (RMW). They probably generate code in which atomic operations are performed with a compare-and-swap (CAS) loop. In our case, this degrades performance. Specifying the flag `-munsafe-fp-atomics` on MI250X, we are specifying to generate assembly code with atomic RMW instructions, but it is not supported on all compilers. Finally, C++ PSTL code achieved an application efficiency of 0.45-0.6 with both `clang++` and `acpp`. This is because we could not properly tune the kernel parameters. Again, we believe that the new executors feature proposed for C++26 could help solve this problem.

C. Code validation

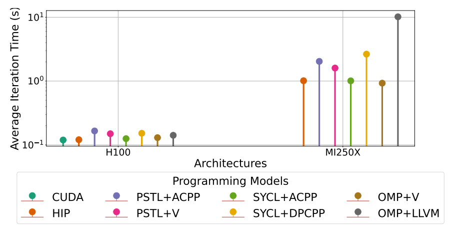
We verified the correctness of the different code versions across all considered frameworks and H100, A100, and AMD MI250x architectures, by comparing the solution of the system from Eq. (2) with its standard error against the solution found by the CUDA code currently in production on the Leonardo supercomputer. For this verification, we consider two real, well-studied datasets of 42 GB and 306 GB. For both datasets, the solution includes the astrometric, attitude, and instrumental



(a) 10 GB Problem

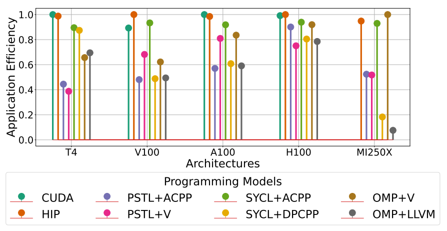


(b) 30 GB Problem

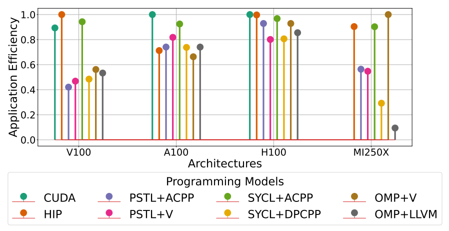


(c) 60 GB Problem

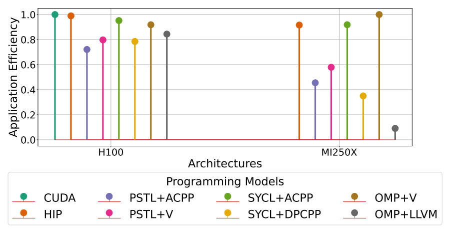
Fig. 4: Average iteration time across architectures and programming models for problems of size: a) 10 GB, b) 30 GB, and c) 60 GB.



(a) 10 GB Problem



(b) 30 GB Problem



(c) 60 GB Problem

Fig. 5: Application efficiency across different platforms and programming frameworks for problems of size: a) 10 GB, b) 30 GB, and c) 60 GB.

sections and no global section, which has not been computed yet in production runs.

The two left panels of Fig. 6 compare the astrometric solution (red) and its standard error (blue) obtained for the 42 GB dataset with the HIP code run on Leonardo and the same quantities obtained with the CUDA-production code on Leonardo as well. The two right panels show the same quantities with the HIP code run on Setonix. The black dashed line testifies the one-to-one relation between the two solutions. Similar results have been obtained on all other considered frameworks for both datasets and, therefore, are not shown. From a visual inspection, we can see that the different quantities are consistent with each other and this agreement is also quantitatively verified, being the different couples of solutions in agreement within 1σ. Moreover, the Gaia mission aims to determine the astrometric parameters with a $10-100$ micro-arcseconds = $(0.48-4.8)\times10^{-10}$ rad precision. We verified that the mean and standard deviation of the differences between the standard errors obtained with the CUDA production code and all other versions always stay below the 10 micro-arcseconds threshold.

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VI. Conclusions and Future Works

Performance portability (Φ) is an increasingly impelling necessity in HPC to lower the time to solutions on new supercomputers. For this purpose, we present a study taking the real-world application AVU-GSR solver, based on the LSQR algorithm, of the ESA Gaia mission as a test case. The main operations are two sparse matrix-by-vector products, a well-known, highly memory-bound operation. Specifically, we optimized the original CUDA version and re-implemented it using HIP, SYCL, OpenMP-GPU, and C++ PSTL, with the purpose of measuring the Φ of each framework across multiple hardware platforms. We considered all the platforms available to us: NVIDIA Tesla T4, Volta V100, Ampere A100 and Hopper H100, and AMD MI250X. We compiled and tested the code using different compilers and verified the correctness of the solutions.

Language-specific programming frameworks, specifically HIP and SYCL, provide the best performance portability values with an average across different problem sizes of 0.94 and 0.93, respectively. CUDA is the best programming framework on NVIDIA architectures, achieving a Φ value of 0.97. OpenMP is the most performant on AMD MI250X when compiled with `amdclang++`. On NVIDIA, the best performance portability values are 0.91 and 0.84 when the code is compiled with `nvc++` and `clang++` on H100, and it is tested on a problem of 60 GB. C++ PSTL achieves its maximum (0.9) application efficiency on H100 and problem sizes of 30 GB and 60 GB. On MI250X, it reaches the values of 0.45-0.6 with both `clang++` and `acpp` compilers. In the Gaia AVU-GSR case, tuning kernel parameters is fundamental to better exploit GPU computational power. Programming frameworks, such as C++ PSTL, for which this is not possible, usually have lower performance portability values. For this reason, using executors, these performance gaps are expected to be reduced.

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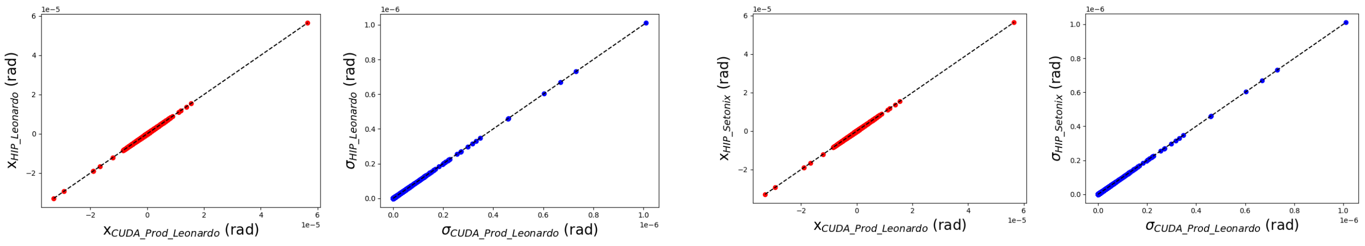

(a) Solution Astrometric (b) Std Error Astrometric (c) Solution Astrometric (d) Std Error Astrometric

Fig. 6: a) Astrometric solution (red) of the system of equations (2), and b) standard error (blue) of the solution obtained on test problem of 42 GB with the HIP code on H100 as a function of the same quantities obtained with the CUDA-production code on Leonardo. The black dashed line represents the one-to-one relation as a reference. c) and d): same plots but with the HIP code executed on MI250X platform.

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APPENDIX A
ARTIFACT DESCRIPTION/ARTIFACT EVALUATION

A. *Overview of Contributions and Artifacts*

1) Artifact repository: https://github.com/alpha-unito/gaia-avugsr-p3hpc

2) Paper's Main Contributions: We measured the performance portability (Φ) of five optimized re-implementations of the Gaia AVU-GSR code written in CUDA, HIP, SYCL, C++ PSTL, and OpenMP with GPU offload (§V-B). We also verified the correctness of the different optimized frameworks against a reference solution (§V-C).

3) Computational Artifacts: The artifact presented in this article is the Gaia AVU-GSR code, which executes the iterative LSQR routine to solve a system of equations (Eq. (2)). The LSQR routines for the different frameworks can be found in the `lsqr_hip.cpp`, `lsqr_stdpar.cpp`, `lsqr_openmp_gpu.cpp`, `lsqr_sycl.cpp`, and `lsqr_cuda.cu` source code files. Each of these routines can be executed by `solvergaiaSim.cpp` solver code, depending on how you compile `solvergaiaSim.cpp`.

Inside the repository, the following artifacts are available:

1) `README.md`: file with the compilation and execution instructions of the code.
2) `LICENSE`: license file with the licence under which the code is released.
3) `Makefile.examples`: Some samples Makefiles to show how to compile the source code for all the different architectures.
4) `src` folder containing all the source code.
   - `solvergaiaSim.cpp`: solver source code.
   - `lsqr_*`: source codes with the different LSQR implementations.
   - `gaiasim_includes`: common headers files
   - other source files
5) `include`: common headers files for the Gaia AVU-GSR application
6) `Scripts`: This folder contains, sorted by used architecture, a sample SLURM script to compile and execute the Gaia AVU-GSR application. Those files are merely examples and must be modified according to the local machine configuration (i.e., compilers' paths and source code's paths must be adjusted accordingly). You will find different folders in the `Scripts` folder (one for each GPU architecture). Inside the architectures folders, two more folders are present:
   - `comp`: Sample SLURM scripts to compile the code, one for each programming framework
   - `test`: Sample SLURM scripts to execute the Gaia AVU-GSR application, one for each programming framework

To better help with the understanding of the GPU architectures and cluster name association, Table IV shows how to interpret the content inside the `Script` folder.

GPU - Cluster reference table	
Cluster name	GPU vendor & model
CascadeLake	NVIDIA V100s
TeslaT4	NVIDIA T4
EpiTo	NVIDIA A100
GraceHopper	NVIDIA H100
Setonix	AMD MI250X

TABLE IV: Cluster name to GPU model reference table

B. *Artifact Identification*

1) Relation To Contributions: Two classes of experiments were performed:

1) In §V-B, we tested the Φ of the five optimized implementations of the solver across five different platforms, four based on NVIDIA GPU architecture (H100, A100, V100 and T4) and one based on AMD GPU architecture (MI250X). The Φ is objectively measured with a metric defined by John Pennycook (Eq. (1)). This test aims to evaluate if the different languages provide portable solutions without a significant performance loss. The results of these tests are illustrated in Figure 3.
2) In §V-C, we validate the correctness of the five optimized implementations of the code against the CUDA version in production, by taking as input two benchmark datasets with a size of 42 GB and 306 GB.

2) Expected Reproduction Time (in Minutes): A single execution of `solvergaiaSim.cpp` (100 iterations with a single version of LSQR among HIP, C++ PSTL, SYCL, CUDA, or OpenMP) should not exceed 5 minutes.

C. *Artifact Setup (incl. Inputs)*

The hardware and software employed in our work are described in §V and Table I.

a) Datasets / Inputs: The datasets used by the Φ are synthetic but distributed in the system as the real data. In the `README.md` file, the instructions on how to run the different tests with an input dataset of a given size are present. The size of the dataset to be passed in input to the system to solve is given at runtime in GB to the executing command of the solver. Once the solver reads this parameter, it randomly generates, given a certain seed, a dataset with the specified size and it runs the solution for 100 iterations, as specified in the scripts in the `Scripts/<target_arch>/test` directory inside the code repository). In these cases, it was not important to obtain the solution at convergence but to measure the iteration time, that 100 iterations proved to be sufficiently stable.

The real datasets used in the code validation section are produced by the ESA Gaia mission and cannot be shared due to a non disclosure agreement, hence motivating the need to provide a synthetic (but mathematically equivalent) dataset to perform tests.

b) Installation and Deployment: To compile the code, gcc version ≥12.2.0 is needed. The compilers used on NVIDIA and AMD architectures are detailed in Table I of the article. Remember to check all the paths inside the compilation scripts to reflect your local installation, particularly the environment variables that define the libraries paths (which are documented inside the scripts), as well as the source code relative and absolute paths inside the scripts and Makefiles.

1) Artifact Execution: We briefly summarize the procedure adopted to execute the tests detailed in §V. The two classes of tests are independent with each other, no output from one test are taken as input to the other test.c

In §V-B, we measured the Ɏ of the five optimized code versions on the five considered platforms with the metric defined by John Pennycook, reported in Eq. (1). The Ɏ results are reported in Figure 3. To calculate the Ɏ, the solver was executed on one GPU of Gracehopper (H100), EpiTo (A100), CascadeLake-V100, CascadeLake-T4, and Setonix, with an input memory set to 10 GB. The same test were executed for an input dataset of 30 GB only on H100, A100, V100, and MI250X and for an input dataset of 60 GB only on H100 and MI250X.

The LSQR was run for 100 iterations. To evaluate the Ɏ, we calculated the "application efficiency" that we derived, in turn, from the "best observed performance" of a specific code version among all the considered platforms. We evaluated the "best observed performance" of each code version as the lowest LSQR iteration time among the considered platforms. We measured the iteration time maximized among all MPI processes and averaged among 100 iterations.