Nuclear Instruments and Methods in Physics Research A 1069 (2024) 169856

Contents lists available at ScienceDirect

Nuclear Inst. and Methods in Physics Research, A

journal homepage: www.elsevier.com/locate/nima

The MIZAR ASIC: 64-channel zone-sampling based ASIC for Cherenkov light detection from sub-orbital and orbital altitudes

Andrea Di Salvo [a,*], Sara Garbolino [a], Marco Mignone [a], Stefan Cristi Zugravel [a,b], Antonio Palmieri [a,c], Angelo Rivetti [a], Mario Edoardo Bertaina [a,c]

[a] Istituto Nazionale di Fisica Nucleare (INFN) - Sezione di Torino, Via Pietro Giuria 1, 10125, Torino, Italy
[b] Politecnico di Torino, Corso Duca degli Abruzzi, 24, 10129, Torino, Italy
[c] Dipartimento di Fisica - Università degli Studi di Torino, Via Pietro Giuria 1, 10125, Torino, Italy

ARTICLE INFO

Keywords:
ASIC
Cosmic rays
Cherenkov light
SiPM
ADC

ABSTRACT

This work describes the implementation of a 64-channel Application Specific Integrated Circuit (ASIC) developed in a commercial 65 nm CMOS technology to readout the signals collected by a camera plane made of Silicon Photo-Multipliers. The aim of the application is the identification of Extensive Air Showers (EASs) by detecting optical Cherenkov light generated by Ultra-High Energy Cosmic Rays (UHECRs) and Neutrinos (UHENUs) from sub-orbital and orbital altitudes. In this context, the ASIC is designed to store each event into an analog memory based on 256 configurable cells per channel. Then the chip forms a hitmap sent to an Field Programmable Gate Array (FPGA) to recognize a pattern of interest. If the signal is externally validated, the digital conversion can occur on-board using an array of 12-bits Wilkinson analog-to-digital converters (ADCs) at 200 MHz of clock. The readout is realized with two serializers running at 400 MHz in double data rate (DDR). Both the number of cells and the resolution can be configured into partitions of 32, 64 or 256 cells and in the range 8–12 bits respectively, becoming a key feature of this ASIC. The chip submission and testing are planned for the forthcoming months.

1. Introduction

The interaction of UHECRs and UHENUs with the terrestrial atmosphere produces EASs and these relativistic particles are characterized by the emission of Cherenkov light. Since the latter is collimated with the direction of the cascade propagation, spatial and energy information of the parent UHECR/UHENU can be tracked detecting this emission. To derive these EAS parameters the light can be collected by a telescope equipped with a focal plane made of a matrix of Silicon Photo-Multipliers (SiPMs). The signal acquired by these sensors from sub-orbital height (~30–40 km) or Low Earth Orbit (LEO, ~500 km) lasts tens of nanoseconds. Simulations show a dependency of this result from the angle subtended between the EAS direction and the axis perpendicular to the focal plane. Due to the durantion of the event, at least a time resolution of the order of 100 MHz is required to adequately process such kind of signals. Moreover, a full waveform sampling system allows to distinguish an EAS-related event from the interaction due to an impinging direct cosmic ray. Table 1 summarizes some requirements for this application.

To satisfy these requirements a 64-channel ASIC is designed taking inspiration from current and future missions in UHECR and UHE neutrino astronomy such as Extreme Universe Space Observatory-Super Pressure Balloon2 (EUSO-SPB2) [1], the planned POEMMA Balloon with Radio (PBR) [2] which is based on a board stratospheric balloon platform, the space-based missions Terzina [3] currently under development and the planned POEMMA [4] mission.

2. ASIC architecture

This section is dedicated to the architecture of the Multi-channel Integrated Zone-sampling Analogue-memory based Readout (MIZAR) ASIC. The design is implemented in a commercial 65 nm CMOS technology with 12 low-voltage differential signaling (LVDS) lines which include a Serial Peripheral Interface (SPI) to configure the ASIC. More in detail, Fig. 1 illustrates a block diagram representation of a channel. The current induced by the sensor is processed with an amplification stage and its output is distributed into two branches. The first feeds a couple of comparators used as trigger of the End-Of-Column (EOC) module. This last module implements the digital control logic of the ASIC merging the information from the channels to generate two

* Corresponding author.
E-mail address: andrea.disalvo@to.infn.it (A.D. Salvo).

https://doi.org/10.1016/j.nima.2024.169856
Received 25 June 2024; Received in revised form 4 September 2024; Accepted 5 September 2024
Available online 10 September 2024

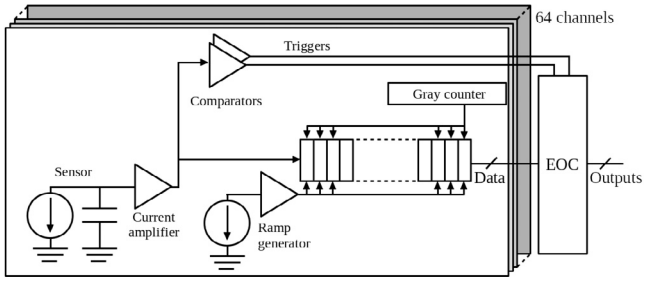

Fig. 1. Block diagram representation of a channel connected with EOC.

Table 1
Summary of application requirements.

Requirement	Value
Die area	(5×6) mm^2
Time resolution	≥100 MHz
ADC resolution	8–12 bits
ADC input range	$0 \div 1$ V
Voltage supply	1.2 V
Power	~5 mW per channel

hitmaps. Since the pixel size is comparable with the size of the point spread function of the optics, a double threshold allows to select the spot contained in one pixel or that one distributed on more pixels. If an event occurs, a read request is sent to an external FPGA. If this signal is accepted, the hitmaps are serialized at 400 MHz in Double Data Rate (DDR). For instance, an interesting pattern could be formed by one pixel over the higher threshold or two adjacent pixels over the low threshold. The second branch connects the output of the amplifier with an array of 256 cells segmented in 8 blocks of 32 cells each. Since the events follow a Poissonian distribution, these 8 partitions ensure the derandomization of the signals [5] realizing the sampling, the digitization and the readout in parallel. Each cell implements a configurable Wilkinson ADC [6] where the waveform is stored in a capacitor (C) during the sampling stage. When the digitization is enabled, the Gray counter and the ramp generator start to operate with the same phase. In this way the conversion takes place in parallel in each unit of the 32-cells partition. When the voltage on the top plate of a unit is larger then a voltage threshold, the value of the Gray counter is locally stored in the cell. The resolution of the converter is programmable in the range [8–12] bits to guarantee enough adaptability for such kind of application where a fine resolution is not mandatory. This represents a key feature since the time saved can be remarkable. Indeed considering the time required for the conversion $2^N T_{clk}$ where N is the number of bits and T_{clk} is the clock period equal to 5 ns, in the case of a full 12-bits resolution the digitization takes around ~20.5 μs while only ~1.3 μs are demanded for the 8-bits configuration. The readout of the data is realized by sending out to the FPGA a stream made of 8-bits header, 6-bits packet information, 16-bits value for internal timestamp, 9-bits addresses, then the converted data of the event.

3. Layout

Fig. 2 shows the layout of a section based on 32 cells which are the building blocks of MIZAR. The area of each cell is (72×9.8) μm^2 and the estimated power is around ~2.5 μW. At the bottom of the leftmost module is located the digital logic of the partition and its domain is separated from the analog one by two substrate lines. This block is assembled with others to form a channel and it is integrated with the EOC. The total area of the chip is (5×6) mm^2 including padring. The ASIC is currently under debugging and mixed-signal simulations are planned in the forthcoming months.

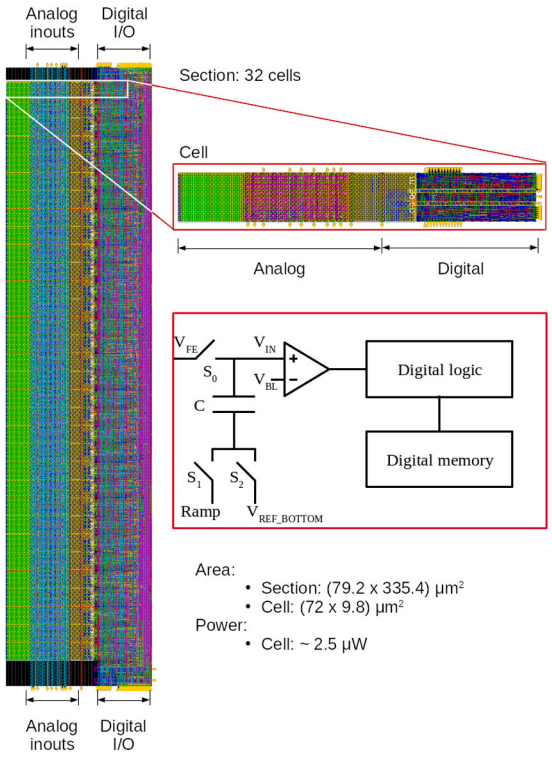

Fig. 2. Layout of a 32-cells partition and physical implementation of a single cell with its schematic.

4. Conclusions

In this work a 64-channel ASIC to readout SiPMs was presented. The technology target of the chip is a commercial 65 nm CMOS node and its channels are partitioned in blocks of 32 cells. Each one is capable of carrying out the sampling, the digital conversion and the readout of the data. The output stream is serialized at 400 MHz in DDR. A MPW production run is planned in the last quarter of this year.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgments

The front-end electronics described in this paper is part of the development performed within ASI-INFN agreement for EUSO-SPB2 n.2021-8-HH.0 and its amendments.

References

[1] J. Eser, A.V. Olinto, L. Wiencke, Overview and first results of EUSO-SPB2, in: 38th International Cosmic Ray Conference, (ICRC2023), 2023, p. 444, http://dx.doi.org/10.22323/1.444.0397.

[2] Matteo Battisti, et al., for the JEM-EUSO Collaboration, POEMMA-Balloon with radio: A balloon born multi-messenger multi-detector observatory, in: 16th Pisa Meeting on Advanced Detectors, 2024.

[3] Leonid Burmistrov for the NUSES Collaboration, Terzina on board NUSES: A pathfinder for EAS Cherenkov light detection from space, EPJ Web Conf. (2023) 283, http://dx.doi.org/10.1051/epjconf/202328306006.

[4] A. Olinto, et al., (POEMMA Coll.), The POEMMA (Probe of extreme multi-messenger astrophysics) observatory, J. Cosmol. Astropart. Phys. (2021) 007, http://dx.doi.org/10.1088/1475-7516/2021/06/007.

[5] Angelo Rivetti, CMOS Front-End Electronics for Radiation Sensors, CRC Press, ISBN: 9781466563100, 2015.

[6] T. Vergine, M. De Matteis, A. Baschirotto, A. Marchioro, A 32-channel 12-bits 65 nm Wilkinson ADC for CMS central tracker, in: 10th Conference on Ph.D. Research in Microelectronics and Electronics, PRIME, 2014, http://dx.doi.org/10.1109/PRIME.2014.6872683.