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SiNAPS: An implantable active pixel sensor CMOS-probe for simultaneous large-scale neural recordings

Gian Nicola Angotzi[a,*,1], Fabio Boi[a,1], Aziliz Lecomte[a], Ermanno Miele[a], Mario Malerba[a], Stefano Zucca[b], Antonino Casile[c], Luca Berdondini[a]

[a] Fondazione Istituto Italiano di Tecnologia (IIT), NetS3 Lab, Genova, Italy
[b] Fondazione Istituto Italiano di Tecnologia (IIT), Optical Approaches to Brain Function, Lab, Genova, Italy
[c] Fondazione Istituto Italiano di Tecnologia (IIT), CTNSC-UniFe, Ferrara, Italy

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ABSTRACT

Large-scale neural recordings with high spatial and temporal accuracy are instrumental to understand how the brain works. To this end, it is of key importance to develop probes that can be conveniently scaled up to a high number of recording channels. Despite recent achievements in complementary metal-oxide semiconductor (CMOS) multi-electrode arrays probes, in current circuit architectures an increase in the number of simultaneously recording channels would significantly increase the total chip area. A promising approach for overcoming this scaling issue consists in the use of the modular Active Pixel Sensor (APS) concept, in which a small front-end circuit is located beneath each electrode. However, this approach imposes challenging constraints on the area of the in-pixel circuit, power consumption and noise. Here, we present an APS CMOS-probe technology for Simultaneous Neural recording that successfully addresses all these issues for whole-array read-outs at 25 kHz/channel from up to 1024 electrode-pixels. To assess the circuit performances, we realized in a 0.18 μm CMOS technology an implantable single-shaft probe with a regular array of 512 electrode-pixels with a pitch of 28 μm. Extensive bench tests showed an in-pixel gain of 45.4 ± 0.4 dB (low pass, $F_{-3\,dB}$ = 4 kHz), an input referred noise of 7.5 ± 0.67 μV_{RMS} (300 Hz to 7.5 kHz) and a power consumption < 6 µW/pixel. *In vivo* acute recordings demonstrate that our SiNAPS CMOS-probe can sample full-band bioelectrical signals from each electrode, with the ability to resolve and discriminate activity from several packed neurons both at the spatial and temporal scale. These results pave the way to new generations of compact and scalable active single/multi-shaft brain recording systems.

1. Introduction

A major challenge in system neuroscience is to understand how complex brain functions are implemented at the neural circuit level (Buzsáki, 2010). To face this challenge, previous works have pointed out the stringent need of proper recording neurotechnologies that are able to monitor with cellular spatial resolution and sub-millisecond time precision both spiking and low frequency bioelectrical signals in large neural networks that span the scale of local brain circuits (see for instance Alivisatos et al., 2013). Filling such a technological gap would be a tremendous step forward in neuroscience (Seymour et al., 2017; Steinmetz et al., 2018) and might provide the technological ground to develop innovative experimental tools to study brain function and dysfunction, to develop therapeutic clinical approaches of interventions or to advance diagnostic instrumentation.

A promising approach to achieve high spatio-temporal resolution recordings of neural activity across large brain circuits (Fig. 1. A) is based on implantable active multi-electrode array (MEA) devices (Steinmetz et al., 2018). The NeuroSeeker (Fiáth et al., 2018; Raducanu et al., 2016) and the NeuroPixels (Jun et al., 2017b) probes have recently demonstrated the use of Complementary Metal-Oxide Semiconductor technology to integrate implantable single-shaft probes (CMOS-probes) with dense arrays of electrodes as well as on-probe circuits for signal conditioning and read-out. As previously shown with planar active devices for *in vitro* electrophysiology (Eversmann et al., 2003; Frey et al., 2010; Hierlemann et al., 2011; Imfeld et al., 2008), CMOS technology allows to overcome spatial constraints on the routing of electrode-pad interconnections that typically limit the electrode

* Corresponding author.
E-mail address: giannicola.angotzi@iit.it (G.N. Angotzi).
[1] Equal contribution.

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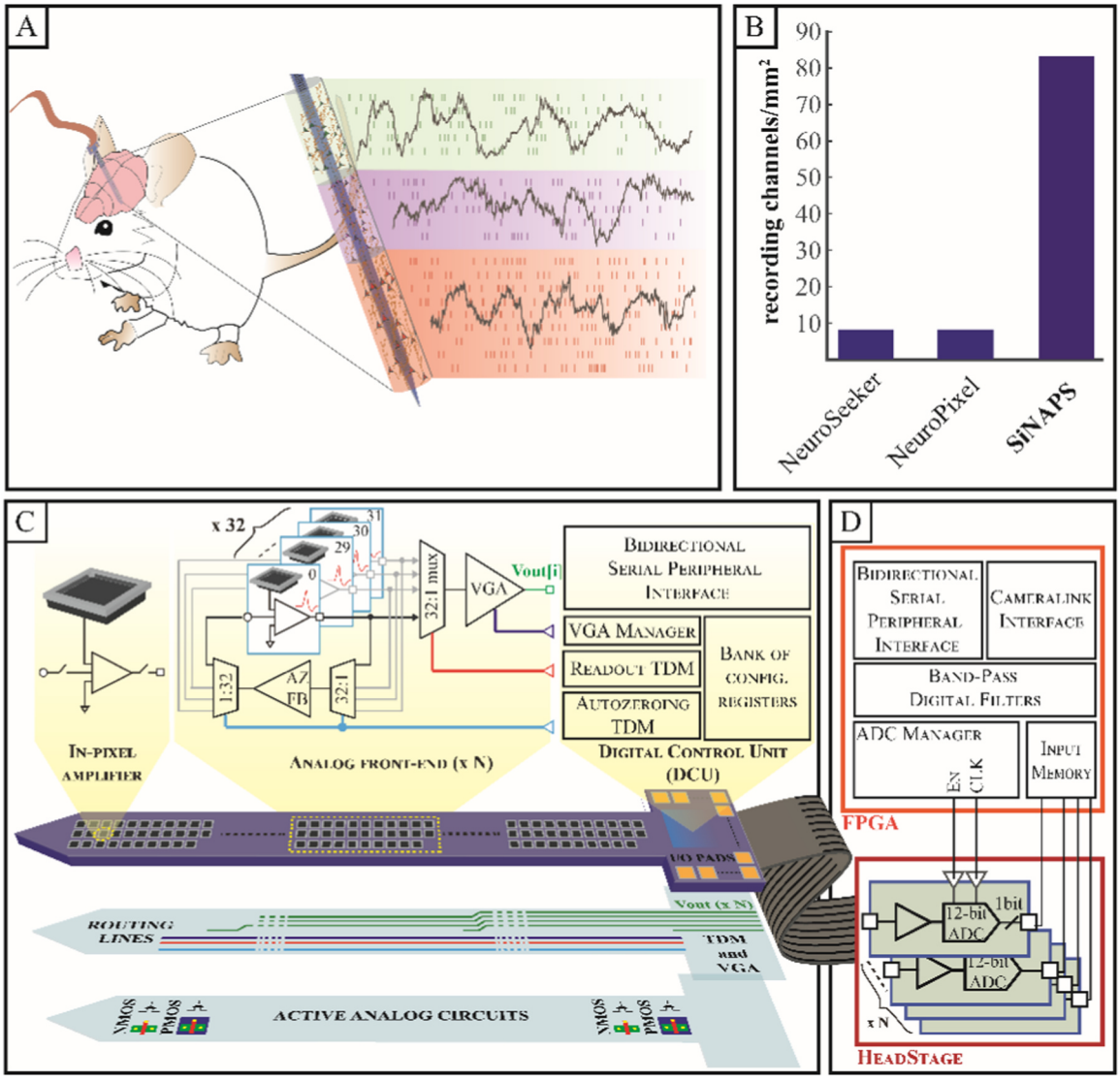

Fig. 1. *Architecture of the SiNAPS probe and of the recording system.* (A) Implantable CMOS probes with dense electrode arrays can record broad-band bioelectrical signals across brain circuits with sub-millisecond and single-neurons resolutions. (B) Comparison of the integration potential of simultaneously recording electrodes (*i.e.* channels) per total silicon area (*i.e.* shaft and base of the probe) for different architectures proposed in the literature. SiNAPS probes achieve a number of effectively recording channels per unit of silicon area that is one order of magnitude larger than other presently available CMOS architectures (NeuroSeeker (Raducanu et al., 2016) and the NeuroPixels (Jun et al., 2017b)). Schematics of the circuit architecture for (C) the SiNAPS probe and (D) its acquisition system providing simultaneous neural recordings from the entire electrode array. Each electrode-pixel features an electrode and a small area DC-coupled in-pixel circuit for local amplification and low-pass filtering. A probe integrates multiple instances of the same low-area and low-power analog front-end module of 32 electrode-pixels that are read out in a time-division multiplexed fashion. The on-probe digital control unit (DCU) provides the timing signals required for correct circuit operation and implements a bidirectional serial peripheral interface (SPI) for device configuration. An FPGA-based acquisition unit generates timing signals for the ADCs and provides a Cameralink standard connection with a PC for data storage and online visualization.

density and number of electrodes in micro-structured passive probes (Berenyi et al., 2014). Further, this approach also allows integrating on-chip front-end circuits for high fidelity and high density extracellular recordings from a large number of microelectrodes. Interestingly, over the last decade two major different circuit architectures were proposed for planar active devices and can be considered for the development of implantable CMOS-probes. The first approach uses on-chip circuits for recordings from sub-sets of electrodes that can be selected from a very large and dense electrode array (Frey et al., 2010; Hierlemann et al., 2011; Müller et al., 2015). In this architecture, an active switching matrix is integrated under the electrode array area while circuits for amplification and filtering are placed outside of the electrode-array area, where constraints on area and power consumption are less stringent, thus permitting circuit design optimization with respect to noise. The second approach is based on the Active Pixel Sensor concept that was originally developed for light-imaging sensors (Fossum, 1997). In this APS-based architecture, the amplifiers are directly implemented underneath each electrode. This design allows continuous whole-array recordings from several thousands of active electrode-pixels (Berdondini et al., 2001; Eversmann et al., 2003; Imfeld et al., 2008), thus permitting to record with sub-millisecond and micrometric resolution the neural activity of large brain regions encompassing several millimeters. In previous work, we validated this approach by developing an APS CMOS-MEA with 4096 electrodes (nowadays commercially distributed by 3Brain AG, Switzerland). The effectiveness of our APS architecture is demonstrated by the large number of *in vitro* studies that used its dense spatial and temporal sampling to track activity propagations and developmental or induced activity changes in cell cultures (Amin et al., 2017, 2016; Berdondini et al., 2009; Dante et al., 2017; Lonardoni et al., 2017; Muthmann et al., 2015; Nieus et al.,

2018), and brain tissues (Ferrea et al., 2012; Hilgen et al., 2017; Maccione et al., 2014; Portelli et al., 2016). Notably, the scalability of the APS approach up to 19,584 simultaneously recording electrodes on planar devices was recently presented (Yuan et al., 2018). However, due to the intrinsic challenges in the design of small area, low-noise and low-power in-pixel circuits, the APS circuit architecture was so far not demonstrated for *in vivo* implantable probes.

Here, we present a novel high-resolution CMOS-probe, - Simultaneous Neural Active Pixel Sensor CMOS-probe (SiNAPS) - designed for whole-array *in vivo* neural activity recordings. First, we describe the circuit architecture and its optimization with respect to noise, size and power consumption. Second, to demonstrate the performances of our in-pixel circuit and APS architecture, we realized, in a standard 0.18 μm CMOS technology, a neural probe that integrates 512 effective recording electrode-pixels arranged in a regular array along a single-shaft of 120 μm in width and 6.5 mm in length (electrode array area of 80 μm × 5 mm). Furthermore, we developed a post-processing workflow based on micro-/nano-fabrication and electrodeposition techniques that allows to make the SiNAPS probe compatible for brain implantation and to modify the native CMOS Al-Cu alloy at the electrode sites with materials adapted to electrophysiological recordings. To control and operate these devices we designed and implemented a complete acquisition platform based on real-time hardware and we adapted in-house available acquisition and analysis software tools, previously developed for *in vitro* electrophysiology with planar CMOS-MEAs. Finally, implantable CMOS-probes were tested mechanically, electrically and electrochemically as well as experimentally *in vivo*. The results presented here demonstrate, for the first time, that the high scalability of our APS-based architecture can be exploited to realize high-density active devices with in-pixel front-end and on-probe time-division multiplexing circuit for *in vivo* neuronal recordings.

2. Materials and methods

2.1. SiNAPS probe architecture

The SiNAPS probe is based on the further optimization of the area and power efficient modular solution that was previously introduced in Angotzi and Berdondini (2015). By integrating multiple instances of such analog front-end module along a narrow and elongated silicon shaft, our CMOS-probe permits acute *in vivo* recordings with sub-millisecond temporal resolution from a high density array of active sensors with *in-situ* amplification and low-pass filtering. As illustrated in Fig. 1. C using the APS concept we developed modules comprising 32 electrode-pixels in which neural data is locally amplified at the recording site and read out in a time-division multiplexed fashion. A variable gain amplifier (VGA) permits further signal amplification (up to 8×) prior to off-chip analog to digital conversion (all characterization results reported in this work were acquired with this gain set to one). The in-pixel circuit provides signal amplification and a first order low pass filter, thus permitting to reduce high frequency noise components and aliasing that might arise from time-division multiplexing readout. Finally, the autozeroing procedure implemented through the operational amplifier *AZ_FB* is used to compensate the DC offset at the electrode-electrolyte interface by periodically adjusting the operating point of the in-pixel amplifier. Differently than in the solution described in Imfeld et al. (2008), for the *in vivo* probe such active feedback loop is shared in a time-division multiplexed fashion among the 32 electrode-pixels of the same module, to optimize both the pixel size and the power consumption for *in vivo* applications. Finally, each electrode-pixel also integrates a NMOS analog switch to provide direct access to the electrode pad by means of a common metal line that is directly routed off-chip. These switches, that are kept open during recording sessions, can be closed for post-processing the sensing electrodes by means of electrodeposition of noble metals or for characterizing the electrochemical impedance of the electrodes (see Section 2.3 for details).

The SiNAPS probe also integrates a digital control unit (DCU) that is used for bidirectional communication with a Field Programmable Gate Array-based (FPGA) acquisition module and for control of device operations. Three distinct operating phases are available: configuration, validation and recording. During the configuration phase a bank of six system registers is loaded with user-defined parameters that set the operating conditions of the device (*i.e.* the variable gain factor, the sampling frequency, the desired readout sequence within each 32 electrode-pixels module and the autozeroing frequency). During the subsequent validation phase the registers are read out for verification purpose only. Finally, the recording phase enables data acquisition with the desired sampling frequency and readout sequence. Each pixel readout can be performed within 1.25 μs, which leads to a maximum sampling frequency of about 25 kHz per electrode-pixel in full readout mode (*i.e.* n times the replication of the 32 electrode module, depending on the probe implementation). The sampling rate can be even further increased by selecting electrode array subsets within each 32 electrode module.

2.2. The back-end module

The back-end module comprises an acquisition unit, a headstage board and a data acquisition software running on a PC equipped with a frame grabber (see Fig. 1. D). The acquisition unit is designed on an Opal Kelly ZEM4310 integration module based on an Altera Cyclone IV FPGA. The unit implements a controller for the analog-to-digital converters (ADCs), an input memory buffer, a bank of programmable band-pass digital filters, a bidirectional interface for communication with the CMOS-probe and, finally, a Cameralink interface for real-time, high-rate data transmission to a PC (similar as in Imfeld et al., 2008).

In this first generation of probes, designed for testing the SiNAPS circuit performances, the multiplexed analog traces produced by the bank of integrated analog front-ends are routed off-chip to the headstage through the I/O pads and buffered before being processed by a bank of analog to digital converters (MAX11105 12 bit, 3Msample/s). Each incoming sample from the ADCs is temporarily stored and, once a new full frame is available (*i.e.* all the available electrode-pixels have been read), it is processed by a bank of programmable band-pass filters operating in real-time on the FPGA. Finally, both raw and filtered data are simultaneously acquired on the PC.

2.3. Post-processing of the SiNAPS probe and electrodes

The CMOS devices were fabricated in a 0.18 μm multi-project-wafer (MPW) CMOS run. Successively, dies with multiple devices were post-processed at the IIT clean-room using photolithograpy and dry micromachining techniques. As depicted in Fig. 2. A, the workflow consists of the following steps. First, a chromium (Cr) layer of 350 nm in thickness is sputtered on the top of the device to obtain an integrated protective mask for the successive etching steps used for shaping the probe (step 1). After photolitography (step 2), the Cr-unmasked regions are etched with an ICP-RIE system (Sentech, Germany), first with a SiO_2/Si_3N_4 etching recipe for approximately two hours (step 3), thus removing completely the SiO_2 (step 4), and then with a standard Si etching Bosch process (step 5). Afterwards, the dies are flipped topside down and Si is uniformly etched from the backside until reaching the final desired thickness of the shaft (step 6). Finally, the devices are cleaned by removing the Cr protective layer and photoresist organic residues (step 7). The resulting structured SiNAPS probes (see Fig. 2. B) are successively wire-bonded on printed circuit boards (PCB).

After chip-mounting, the native CMOS Al-Cu alloy metal at the electrode sites is modified by platinum (Pt) electroplating. Besides improving the electrochemical stability, coating of the electrodes can also significantly decrease the electrochemical impedance, thus reducing the thermal noise contribution of the electrode itself (Hassibi et al., 2004). Interestingly, the coating can also contribute to some extent to

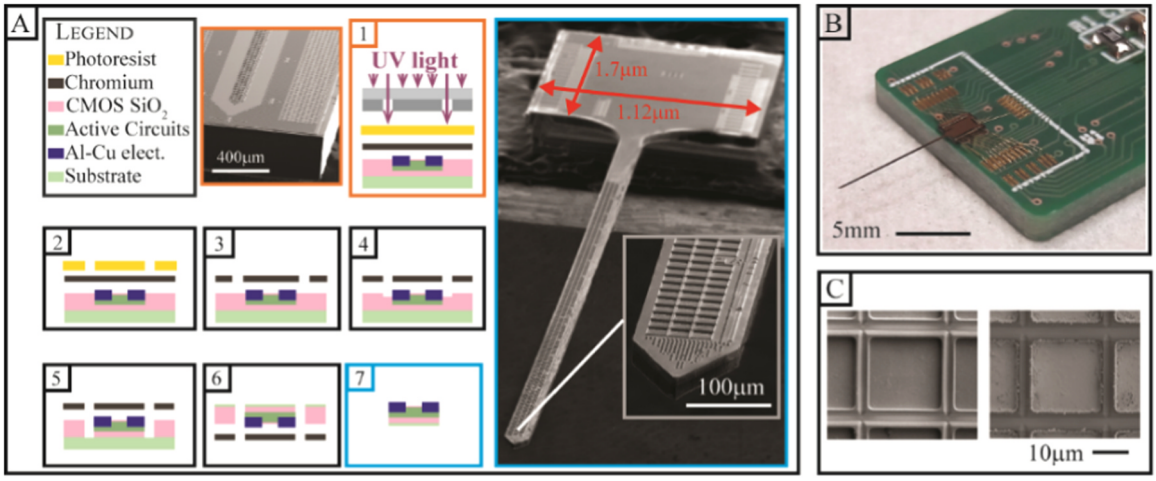

Fig. 2. *Post-processing of SiNAPS probes*. This includes steps for shaping and thinning the probe (see Section 2.3), mounting it on a printed circuit board (PCB) and depositing adapted electrode materials for neurointerfacing. (A) workflow of the microfabrication process (steps 1–7) with SEM images showing a detail of the SiNAPS probe (tip of the shaft) as received from the foundry (thickness of 315 μm) and at the end of the structuring process (shaft final dimensions of L × W × T = 6.5 mm × 120 μm × 30 μm). (B) Structured CMOS-probes are wire-bonded on a PCB. Wires are further protected with an epoxy glue (not shown). (C) The native Al-Cu CMOS alloy (left side) of the sensing electrodes (size of 20 μm × 20 μm) is electroplated with platinum to reduce the electrode impedance and ensure low-noise and stable neural interfacing.

improve the signal to noise ratio by reducing the cleft between the tissue and the electrode (Graham et al., 2009). For a first validation of these probes we used Pt since it is well-known to be a biocompatible and stable material for neural interfacing. For the electrochemical measures we used a potentiostat/galvanostat (PGSTAT204, Metrohm Autolab, Switzerland) equipped with a module for impedance analysis (FRA32M Module, Metrohm Autolab, Switzerland). These measures were performed using a three-electrodes configuration. In particular, all electrode-pixels of the SiNAPS probe were short circuited and were used as the working electrode (WE); a Pt wire was used as the counter electrode (CE) and, finally, a Ag|AgCl|KCl (3 M) commercial electrode (model 6.0733.100, Metrohm, Switzerland) as reference electrode (RE). Solutions were de-aerated by bubbling N2 for 20 min prior to all electrochemical experiments. After removing the native aluminum oxide in Al_2O_3 wet etchant (H_3PO_4:H_2O:CH_3COOH 20:5:1, 10 min), Pt electroplating was performed through Cyclic Voltammetry (5 cycles, from −1.2 V to −0.5 V) in a commercially available Platinum solution (PLATINUM AP + 4G/L, from Italgalvano). The resulting Pt layer ensures a good adhesion with the native Al-Cu alloy and provides a rough texture at the microscale (see left side of Fig. 2. C).

2.4. Electrical, electrochemical and mechanical tests

The electrical and electrochemical properties of SiNAPS probes were validated with measures performed in a Faraday cage and in phosphate buffered saline (PBS) solution to contact the sensing electrodes. The gain frequency response was evaluated by injecting with a Pt wire immersed in the PBS solution pure sine waves of different frequencies and constant amplitudes. Similarly, the intrinsic noise of the system was measured with the PBS bath forced to the reference voltage of the acquisition system. Also, electrochemical impedance spectroscopy (EIS) was performed in NaCl 0.9% solution at ten frequencies per decade over the range 10^1–10^5 Hz (PGSTAT204, Metrohm Autolab, Switzerland). The impedance value for the single electrode was estimated as 512× larger than the one measured with all the 512 sensing electrodes connected in parallel. For mechanical tests, an experimental setup consisting in an adapted Detkat Stylus profiler was used. By means of the 5 μm radius stylus, forces spanning from 1 mg to 5 mg were applied to the backside of the structured probes (50 μm thick) and the corresponding deflection was measured for each point while scanning on the backside surface of the probe shaft along its 6.5 mm length (resolution of 0.33 μm/sample). Such deflection curves (*i.e.* vertical displacement in the direction parallel to the applied force and orthogonal to probe axis) were finally used to calculate the average Young's modulus (Melorose et al., 2015). Finally, the temperature of the probe under constant operation was evaluated with a 320×240 pixel resolution infrared camera (T460, FLIR Systems, inc., Wilsonville, OR, USA). Thermal images of the SiNAPS probe running at 25 kHz/channels sampling rate were taken after one hour of continuous operation.

2.5. In vivo neural recordings

In vivo acute recordings were carried out on an adult anaesthetized Sprague Dawley rat in accordance with the guidelines established by the European Communities Council Directive (license number 332/2015-PR). The rat was anaesthetized with a mixture of Xylazine (5 mg/kg) and Ketamine (30 mg/kg) and positioned on a stereotaxic frame. A small craniotomy was performed (AP −3.5 mm, ML 3.5 mm) in order to expose a small portion of the somatosensory cortex. The SiNAPS probe was lowered, without removing the *dura*, along the dorso-ventral axis at 3 mm depth. A small Pt wire acting as pseudo-reference for the neural probe was attached to a surgical screw fastened to the frontal side of the skull and in contact with the cerebrospinal fluid.

3. Results

3.1. System design and CMOS post-processing

In this work, we describe SiNAPS (Simultaneous Neural Active Pixel Sensor CMOS-probe), a novel circuit architecture for brain implantable high-density active probes with on-probe front-ends and time-division multiplexing circuits capable of whole-array recordings up to 1024 micrometer-spaced electrodes at 25 kHz/electrode. The SiNAPS neurotechnology exploits the Active Pixel Sensor (APS) concept to define a regular array of electrode-pixels with the first-stage low-pass amplifier underneath each electrode. This design allows to avoid the integration of large-area amplifiers at the base of the probe and to minimize the total CMOS Si area (shaft and base) of the probe. Indeed, as shown in Fig. 1. B, we estimate that this solution achieves a number of recording channels per total silicon area of the probe that is almost an order of magnitude higher than the currently available NeuroPixels and NeuroSeeker architectures (*i.e.* 83 channels/ mm^2 vs ≈8 channels/mm^2).

Notably, these figures are based on a worst-case overestimation of the Si area that the SiNAPS would have if it included, similar to NeuroPixels and NeuroSeeker, circuits for analog to digital conversion. Specifically we considered the worst-case Si area required by 16 ADCs and by using the layout of an ADC (1 Msample/s, 10 bit) developed in 0.35 μm CMOS technology that we previously presented for a multi-probe synchronous neural recording system (Angotzi et al., 2018). Given the fact that our SiNAPS probe is designed in a 0.18 μm technological node, this can be considered as a fair overestimation of the Si area that would be required for the integration of an ADC for each 32-electrode-pixels module.

To demonstrate and characterize the performances of this APS circuit architecture we realized, in standard 0.18 μm CMOS technology and using micro-/nano-structuring and electrochemical post-processing, an implantable CMOS-probe with a dense array of 512 recording channels. The active sensing area of the probe was designed by replicating along a narrow and elongated shaft, multiple (16×) instances of a low-power and low-area analog front-end module of 32 electrode-pixels. This spatial arrangement defines a regular 3-columns array of 512 electrode-pixels (pitch of 28 μm and electrode openings of 20 μm × 20 μm) that are read out in a time-division multiplexed fashion followed by an off-probe 12 bit analog-to-digital conversion at the headstage level and data acquisition on a PC *via* an FPGA-based data acquisition and control board (see Fig. 1 C-D). We specifically optimized the electrode-pixel design and the DC-coupled in-pixel circuit (Berdondini et al., 2001; Imfeld et al., 2008) for *in vitro* electrophysiology, achieving a total circuit area of 330 μm × 120 μm for each complete module (*i.e.* electrodes, in-pixels circuits, off-pixel auto-zeroing and time-division multiplexing circuits). Each SiNAPS probe also integrates a digital control unit at its base that provides the timing signals required for correct operation of the device and implements a bidirectional communication with the FPGA board.

To make the devices implantable, we used Si-machining clean-room processes (see Fig. 2). Single dies with multiple CMOS-probes, produced in multi-project-wafer CMOS runs (MPWs), were shaped to a shaft-like geometry (shaft width of 120 μm and 6.5 mm in length) and thinned to a final thickness of either 30 μm (for final *in vivo* implantation) or 50 μm (for initial tests). After mounting and wire-bonding the probes on small PCBs (see Fig. 2. B), we also modified the native Al-Cu CMOS alloy (99.5% Al, 0.5% Cu) of the electrode sites using, as a first step, electrochemical Pt deposition (Fig. 2. C) and by exploiting on-probe circuits that allow to access the electrodes for electrochemical deposition and characterization.

3.2. Electrical, electrochemical and mechanical performances

In line with our design specifications, the in-pixel low-noise front-end circuit operates as a low-pass filtering amplifier ($F_{-3\,dB}$ = 4 kHz) with a gain of 45 ± 0.4 dB across all 512 simultaneously recording electrodes (Fig. 3. A). The distribution and the average noise for the 512 simultaneously recording electrodes operating at a sampling frequency of 25 kHz/channel is reported in Fig. 3.B. The measured input referred noise accounts for 24.5 ± 4.1 μV_{RMS} in the 1 Hz to 1 kHz band and it reduces to roughly 7.5 ± 0.67 μV_{RMS} in the 300 Hz to 7.5 kHz band. Notice that in the low frequency band the noise is dominated by the 1/f noise contribution of the in-pixel amplifier while, at higher frequencies, the noise is mostly thermal and includes the contribution of the electrode-electrolyte interface. These values were measured on CMOS-probes with electrodes having an average electrochemical impedance reduced from 14 ± 0.6 MΩ/electrode at 1 kHz in saline (0.9% NaCl) for the native CMOS metal, down to 529 ± 128 kΩ/electrode upon Pt electrodeposition (see Fig. 3. C).

Furthermore, we measured a worst-case power consumption (*i.e.* all circuits constantly ON) of 6 μW per recording channel, with a supply voltage of 1.8 V. Under normal operating conditions, this worst-case value is reduced by roughly 30% by the power scheduling techniques implemented in our system, which place in standby-mode the majority of the circuits when they are not needed. These very low-power conditions meet the power dissipation constraints posed by *in vivo* recording conditions. Notably, even after one hour of continuous operation, the probe showed no appreciable increase in temperature (Fig. 3. D). Finally, we quantified a Young's modulus of 50 GPa for a 50 μm thick probe shaft (see Fig. 3. E) and we observed, during *in vivo* preliminary experiments, that the mechanical properties of devices with thicknesses down to 30 μm allowed multiple insertions of the same probe in the brain without noticeable damages.

3.3. In vivo neuronal recordings

To quantify the functional characteristics of our device, we performed acute recordings from different regions of the somatosensory cortex area of an anaesthetized rat. After penetrating the *dura* we lowered the SiNAPS probe down to a depth of 3 mm from the cortex surface, resulting in roughly 320 electrodes collecting broad-band (1–7500 Hz) neural activity from the somatosensory cortex as well as the underlying hippocampus (Fig. 4). Recorded Local Field Potentials (LFPs) showed average amplitudes of about 800 μV_{pp} while action potentials (AP) up to 500 μV_{pp} were identified by hard-thresholding the neural traces filtered in the AP band (threshold set to 4.5× the signal RMS with a refractory period of 2 ms and artifact rejection for signal amplitudes larger than 1 mV).

A notable feature of high-density probes is that they can potentially record the same unit cross multiple nearby electrodes. This redundancy in the recorded signals can be exploited to improve the spatio-temporal discrimination of multiple neurons. To investigate this capability, we analyzed the spiking neural activity recorded during the same experimental session. For example, visual inspection of signals collected from 30 neighboring electrodes located in the hippocampus clearly shows contributions from multiple single-units. A more fine-grained analysis of their spatio-temporal response pattern and autocorrelograms allowed us to isolate the contributions of three distinct single units (see Fig. 5. A). This result is further confirmed in Fig. 5. B, that shows that the correlation coefficients computed among the spike trains of the different units are close to zero ($Corr_{12}$ = 0.043, $Corr_{13}$ = 0.075, $Corr_{23}$ = 0.036). Finally, we also represented each spike in a three-dimensional space by considering its negative peak amplitude (NPA), negative peak duration (NPD) and peak-to-peak amplitude (PtoP) (see Fig. 5. C). K-means clustering of these data points further confirmed the presence of three distinct units.

4. Discussions

Active high-density multi-electrode array probes offer the unprecedented capability to record wide-band bioelectrical signals from potentially large brain regions with high spatial and temporal resolution and they are opening new exciting directions in systems neuroscience (Seymour et al., 2017; Steinmetz et al., 2018). In this work, we present a novel scalable circuit architecture, based on the Active Pixel Sensor concept, and we validate it for the first time with *in vivo* recordings.

4.1. The SiNAPS circuit architecture for in vivo neural recordings

The circuit design of active bioelectronic devices for brain interfacing requires minimizing three distinct yet closely related figures of merit, namely, noise, Si area and power consumption. Extracellularly recorded neuronal spikes have typical amplitudes ranging from tens to hundreds of μV and with most of their energy below 5 kHz. Thus, low-noise amplification is mandatory and low-pass filtering is required to cancel high frequency noise components. Additionally, large DC fluctuating offsets arising from the electrode-electrolyte interface need be removed to prevent saturation of the amplifiers. While these

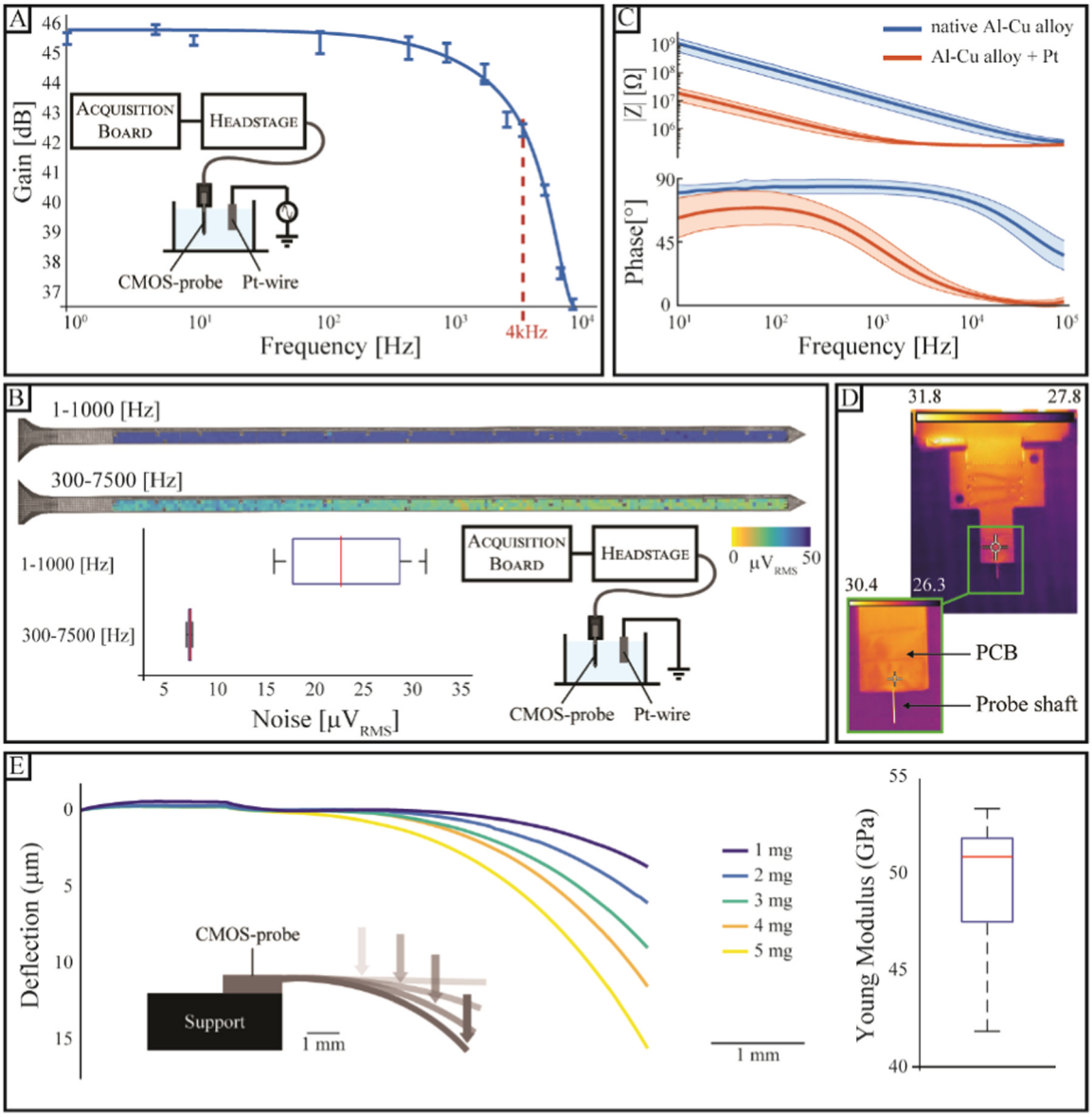

Fig. 3. *Electrical, electrochemical and thermal characterization of the 512-electrodes SiNAPS probe.* (A) Gain-frequency response of the in-pixel amplifier measured for the 512 electrode-pixels working simultaneously. The blue curve represents the average response across all 512 electrode-pixels working simultaneously and vertical bars represents standard error. For this test, the SiNAPS probes were dipped into a beaker containing phosphate-buffered-solution (PBS) where pure sine waves of different frequencies and with constant amplitudes were injected using a Pt wire. (B) Input referred noise for the whole CMOS-probe electrode-pixels array measured separately in the low- (1–1000 Hz) and high- (300–7500 Hz) frequency bands. For this test, the PBS bath was forced through a Pt wire to have the same reference voltage of the SiNAPS probe. The color maps show RMS noise values across the entire 512 electrode array. The box plot indicates a noise of 24.5 ± 4.1 μV_{RMS} and 7.5 ± 0.67 μV_{RMS}, in the 1 Hz to 1 kHz and 300 Hz to 7.5 kHz frequency bands respectively. (C) Electrochemical impedance (module and phase) averaged for a single electrode before and after Pt electrodeposition (performed on n = 6 probes). The impedance module reduced from 14 ± 0.6 MΩ/electrode at 1 kHz for the native CMOS metal, down to 529 ± 128 kΩ/electrode upon Pt electrodeposition. (D) Thermal picture of one SiNAPS probe after one hour of continuous operation. (E) (left) Measured vertical deflection produced by the application of different forces (1–5 mg) on the backside of a 50 μm thick probe shaft. The mean Young's modulus at the tip of the probe (right) was derived by averaging deflections across the different applied forces. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

requirements apply to any neuronal recording technology, either passive or active, they become stringent and hard to meet in active CMOS-probes where the high degree of integration (*i.e.* the number of recording sites per unit of area) can produce potential heating issues. Indeed, brain tissue is very sensitive to heat and to avoid excessive local temperature increases, implantable devices have to dissipate less than 40 mW (Marblestone et al., 2013).

Therefore, in order to exploit the area effective and scalable APS circuit architecture for implantable neural interfaces (Seymour et al., 2017), an important challenge of this work was the development of a low-power, low-area and low-noise APS-based in-pixel circuit for local amplification and filtering underneath each electrode, before time-division multiplexing. Following Harrison and Clark's original proposal (Harrison and Charles, 2003), many AC-coupled input stages for the removal of DC offsets across differential electrodes have been proposed in the literature. Unfortunately, these solutions are not suitable for an APS architecture as they would require large area in-pixel capacitors. For this reason, similarly to our previous work (Imfeld et al., 2008), the SiNAPS probe implements a more area-efficient solution consisting in an active feedback loop that periodically cancels DC differences across differential electrodes. This solution allowed not only to integrate a DC-coupled low-pass amplifier capable of recording wide-band

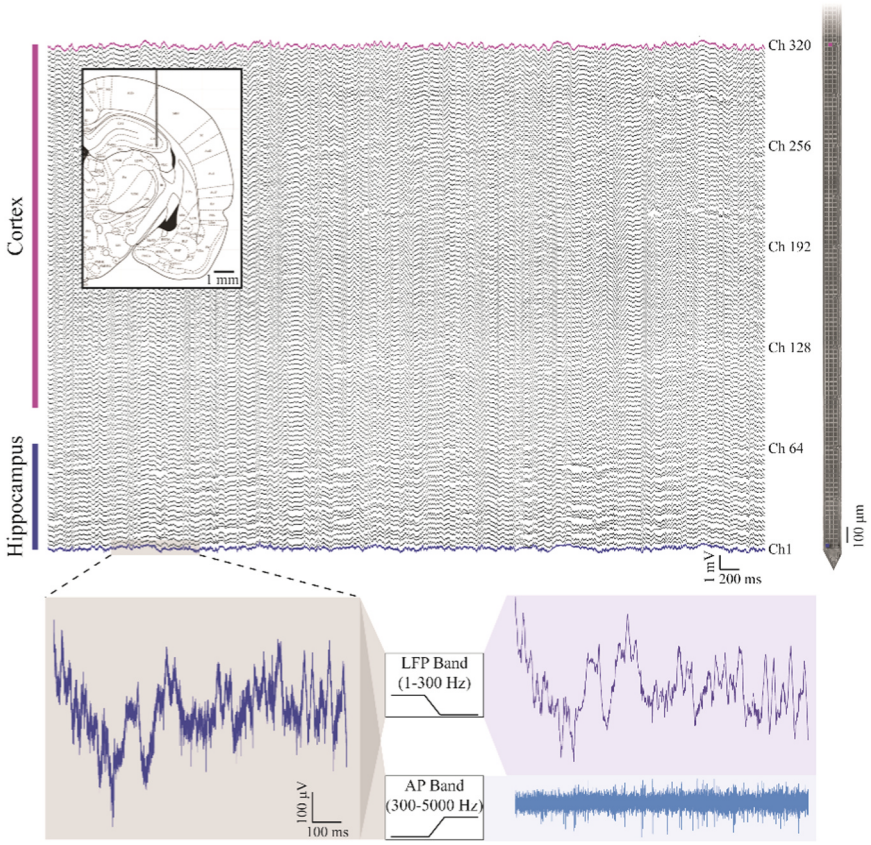

Fig. 4. *Example of in vivo neural activity recordings.* (top) Neuronal signals simultaneously recorded from the electrode array of a SiNAPS probe implanted in the brain of an anaesthetized rat (location indicated in the top-left inset). The curves represent full-band bioelectrical signals recorded from the somatosensory cortex down to the hippocampus (time window of 7 s). We recorded physiologically-related signals from a total of 320 electrodes. To avoid cluttering we show only a subset of 110 of them (pitch of 28 µm). (bottom) Close-up of a representative single raw neural trace recorded in the hippocampus (left) and off-line filtered in the LFP (1–300 Hz) and AP (300–5000 Hz) frequency bands (right). Abbreviations: AP, Action Potential; LFP, Local Field Potential.

physiological signals (LFPs and APs) in a pixel size of only 26 μm×26 μm, but also to meet noise and power constraints. Indeed, extensive testing of the circuit shows a DC gain of 45 dB, a first order roll-off at 4 kHz and an input-referred noise of 7.5 μV_{RMS} in the AP-band. This low level of noise was mandatory for *in vivo* recordings and was obtained by optimizing all in-pixel components to minimize their thermal noise contributions in the AP-band and the 1/f noise contributions dominating the LFP-band. Importantly, the in-pixel low-pass filtering circuit permits to relax aliasing resulting from time-division multiplexed readouts from the whole array. Furthermore, the 512-electrode SiNAPS probe used in this work consumes less than 3 mW of total power. This value is well below the safety limit of 40 mW used in *in vivo* recordings, thus allowing to further increase the number of simultaneously recording channels in future generations of SiNAPS probes.

The electrical and electrochemical performances of the SiNAPS probe allowed to record in acute experimental conditions wide-band bioelectrical signals, including LFPs and APs, from the brain of an anaesthetized rat, throughout cortical and hippocampal areas. To do so we realized a 512-electrode APS CMOS-probe with the specifications reported in Table 1. The acquired experimental data validate this circuit solution and demonstrate the capability of exploiting APS architectures for continuous recordings from dense electrode arrays to identify and spatiotemporally map the spiking activity of multiple units from both cortical and sub-cortical brain structures.

4.2. Comparison with other high-density CMOS-probes

The SiNAPS probe circuit architecture advances current state-of-the-art high-density active probes in several key directions (see Table 1 for comparison). In particular, it permits simultaneous readouts from all electrode-pixels in the array while minimizing the total Si-area. As shown, in Fig. 1. B, SiNAPS probes can reach a number of effectively recording channels per unit of silicon area that is almost one order of magnitude larger than present state-of-the-art devices. This is important to minimize the production cost of the devices as well as for the further development of this technology toward compact chronically implantable devices. Furthermore, as shown in Fig. 5, dense neuronal recordings combined with modern spike sorting algorithms (Hilgen et al., 2017; Jun et al., 2017a; Yger et al., 2018), can exploit spatial and temporal correlations between signals recorded from nearby electrodes, to provide a virtually noise-free readout of neuronal responses.

Two other circuit architectures for dense recordings have been presented in the literature: The NeuroPixels and the NeuroSeeker probes. The NeuroPixels probe (Jun et al., 2017b) implements a circuit architecture for a sub-array readout strategy in which each pixel amplifier along the shaft merely implements *in situ* buffering circuits while the actual signal amplification and filtering is performed at the base of the probe, only for a limited subset of preselected recording sites. Thus, the number of effectively available channels is sensibly lower than the number of electrodes present on the probe and this architecture permits integrating large front-end amplifiers to reduce their input referred noise. The NeuroSeeker probe (Raducanu et al., 2016) implements a time-division multiplexed readout that overcome this problem and allows whole array readouts. This architecture lacks however the in-pixel low-pass filters that are present in the SiNAPS probe, and it thus requires a complex and large-area circuit to reduce noise components folding into the signal band. Overall, in both state-of-the-art solutions, the complexity either of the routing circuitry along the shaft or of the circuit architecture strongly limits the scalability. Thus, this imposes larger minimal sizes that imply higher CMOS production costs. Furthermore, results presented here show that, despite of their smaller circuit size, our front-end circuits achieve noise levels that are comparable to those of the NeuroPixel probe in the AP-band and slightly higher in the LFP-band, primarily due to larger 1/f noise contributions.

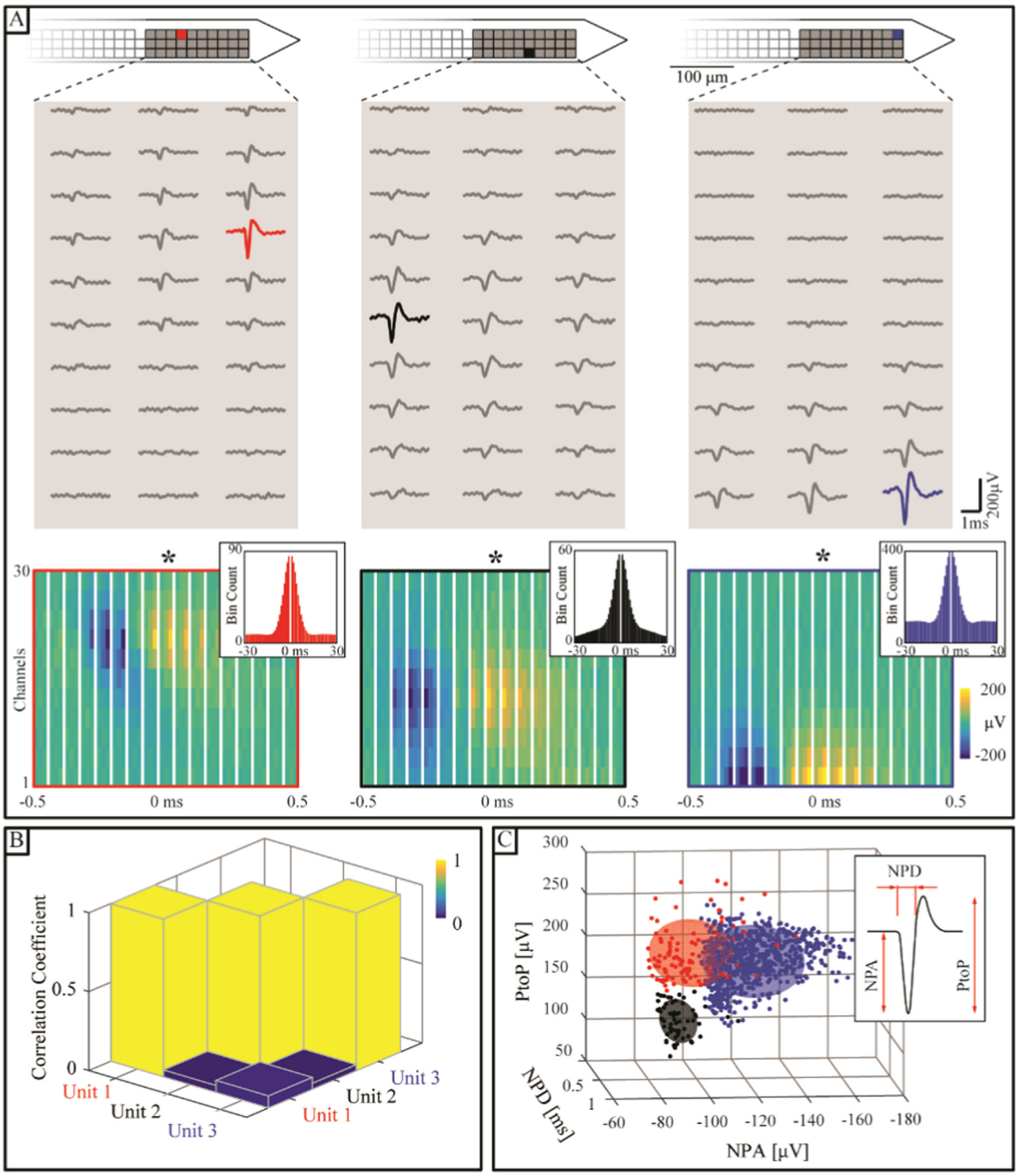

Fig. 5. *Multiple single-neuron spikes can be spatio-temporally mapped and separated.* (A) (upper panel) Example of mean action potential (AP) waveforms recorded from 30 nearby electrodes (pitch of 28 μm) located in the hippocampus. The gray area on the probe represents the sites considered to compute the mean. The colored squares indicate electrodes where the largest peak-to-peak signal was recorded (in red Unit1, in black Unit2 and in blue Unit3). (lower panel) The bidimensional maps show the spatio-temporal evolution, across the 30 considered electrodes, of the extracellular potential for each of the three units. $t = 0$ indicates the time of the maximum positive peak of each AP occurrence and the inset shows the autocorrelograms for the spike-trains of each unit (bin size: 1 ms). (B) Correlation coefficient between the spike trains recorded from the electrodes highlighted in panel A. (C) Three-dimensional representation of the waveform features (*i.e.* Negative-Peak Amplitude (NPA), the Negative-Peak Duration (NPD) and the Peak-to-Peak Amplitude) for all APs recorded from the same three electrodes. Each dot represents a single spike in the 3D feature space and its color shows its assignment to one of the three units based on a K-means classifier (colored ellipsoids). (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

4.3. Challenges and future directions

The results presented in this work pave the way to the exploitation of the modularity of the SiNAPS technology to develop CMOS probes with different layouts and geometries tailored to different experimental needs and applications. This may include multi-shaft probes that further extend the spatial recording capabilities to larger areas; compact and fully integrated implantable devices that can interconnect large bundles of micro-wires for long-term chronic implants (Guitchounts et al., 2013); or CMOS-probes with smaller shaft widths to minimize tissue reactions for chronic implants. Notably, the sensing capabilities of our CMOS-probes can be further improved by exploiting other electrode materials such as CNTs (Baranauskas et al., 2011; Keefer et al., 2008), graphene (Fabbro et al., 2016; Reed, 2014) or PEDOT: PSS (Khodagholy et al., 2016; Malliaras, 2010). This can be studied either by exploiting the on-probe circuits that we used to access the electrodes

Table 1
Comparison with the State-Of-The-Art.

	NeuroPixels	NeuroSeeker	**SiNAPS**
Amplifier	On base (AC-input)	In-pixel & on base (AC-input)	**In-pixel (DC-input)**
ADC	On-chip (10 bit)	On-chip (10 bit)	**Off-chip (12 bit)**
Sampling Freq.	30 kHz	40 kHz	**25 kHz**
TDM	On the base (after ADCs)	On-probe	**On-probe**
Shaft (L·W·T) [μm^3]	$10 \cdot 10^3$ x 70 x 20	$8.15 \cdot 10^3$ x 100 x 50	**$6.5 \cdot 10^3$ x 120 x 30**
Base (L·W) [mm^2]	8 x 5 (estimated)	12.9 x 13.5	**1.7 x 1.12**
Electrodes/channels	960/384	1344/1344	**512/512**
RMS noise [μV]	5 (0.3–10 kHz)	31 (0.3–7.5 kHz)	**7.5 (0.3–7.5 kHz)**
	9 (0.5 Hz to 1 kHz)	125 (1 Hz – 1 kHz)	**24.5 (1 Hz – 1 kHz)**
Power	NA	63 μW/pixel	**< 6 μW/pixel**
	NA	45 μW/out ch.	
CMOS Process	0.13 μm	0.13 μm	**0.18 μm**
Electrode Material	TiN (CVD)	TiN (CVD)	**Pt (electrodep.)**

for electrodeposition or by developing adapted post-processing. In this regard, the exploitation of multi-project-wafer CMOS runs (MPW) as well as post-processing methods established in this work will allow evaluating different CMOS-probes before increasing their volume production using wafer-level processes.

The ultimate goal of our work is to produce probes that can be chronically implanted in free-moving animals. To this end, the roadmap that we presently see involves the integration of on-probe analog-to-digital converters, digital multiplexing circuits and high-data rate wireless interfacing circuits (see for instance Crepaldi et al., 2018), together with implantable powering and device packaging solutions.

5. Conclusion

In summary, we have demonstrated the realization of miniaturized high-density brain implantable CMOS-probes with a circuit architecture based on the Active Pixel Sensor concept. This approach provides advantages in CMOS silicon area minimization, while ensuring unique whole-array simultaneous recordings at low-noise and low-power consumption from hundreds to several thousands of closely spaced microelectrodes. The modularity and the performances of the SiNAPS technology described here can pave the way for a new generation of highly integrated implantable probes that can be adapted to different animal models and applications. Future work needs to improve the SiNAPS architecture for monitoring spontaneous or evoked neural activity in freely behaving animals. This step requires facing design challenges related to the optimization of the probe's wiring, materials, packaging and geometry.

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