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Charge sensing properties of monolithic CMOS pixel sensors fabricated in a 65 nm technology

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ABSTRACT

In this work the initial performance studies of the first small monolithic pixel sensors dedicated to charged particle detection, called CE-65, fabricated in the 65 nm TowerJazz Panasonic Semiconductor Company are presented. The tested prototypes comprise matrices of 64 × 32 square analogue-output pixels with a pitch of 15 μm. Different pixel types explore several sensing node geometries and amplification schemes, which allows for various biasing voltage of the detection layer and hence depletion conditions and electric field shaping. Laboratory tests conducted with a ^{55}Fe source demonstrated that the CE-65 sensors reach equivalent noise charge in the 15 to 25 e^- range and excellent charge collection efficiencies. Charge sharing is substantial for standard diodes, but can be largely suppressed by modifying their design. Depletion of the thin sensitive layer saturates at a reverse diode bias of about 5 V.

1. Introduction

Monolithic CMOS pixel sensors have become a key technology for the high energy physics detectors and recent roadmaps [1,2] foresees their further development. Decreasing the CMOS process feature size is expected to enhance their overall performance, in terms of time and spatial resolutions, power dissipation and hit handling capabilities. CERN has organized the access to the 65 nm TowerJazz Panasonic Semiconductor Company (65 nm TPSCo) process, which is currently investigated by a large consortium as a potential technological candidate for the design of sensors to be used in various future detectors, the closest in time being the ALICE-ITS3 project [3].

This paper covers both a report on the design as well as the early characterization of several test pixel matrices implemented in sensor prototypes named CE-65 and fabricated during the first submission of the aforementioned consortium.

2. Design overview

The CE-65 detectors family was designed to explore the charge collection properties of the 65 nm TPSCo process. It consists of four different chips equipped with exactly the same readout electronics, but featuring two pixel pitches (15 and 25 μm) and various sensing node geometries. This work includes studies on two of them, called further

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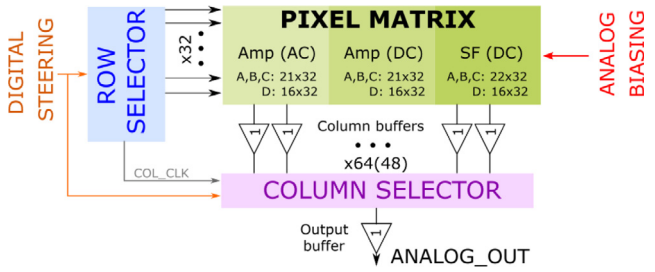

Fig. 1. High level functional block diagram of CE-65 showing the arrangement of the different in-pixel electronics parts.

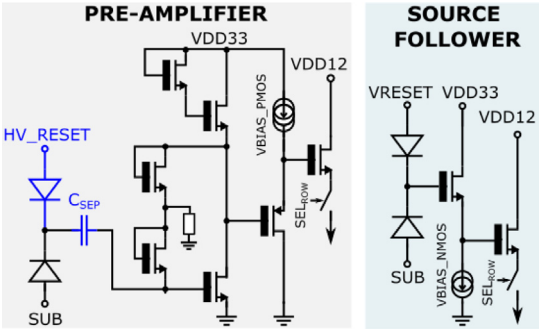

Fig. 2. Schematic of source follower in-pixel circuitry (right) and DC preamplifier (left). AC preamplifier scheme is analogous with AC coupling added (blue).

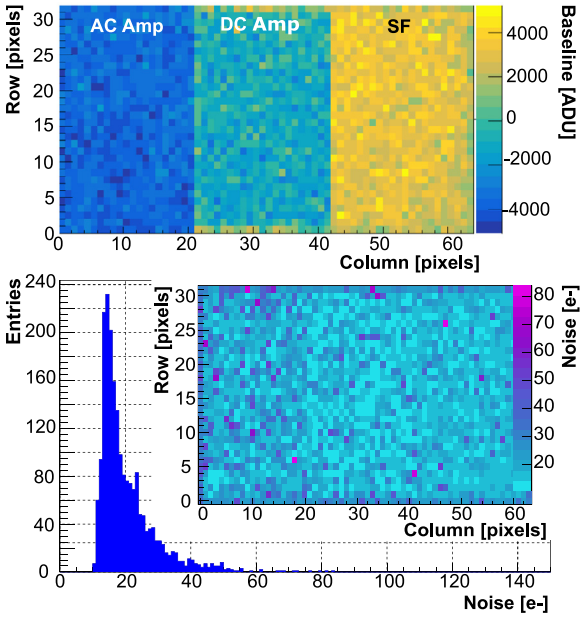

Fig. 3. Baseline (top) and noise (bottom) distributions for the basic diode.

basic and optimized diode, both with 15 µm pitch. The first variant implements a standard small collection well, being a reference sensing diode structure. The optimized diode is a modification following ideas introduced in [4] and targets the development of a lateral electric field at the pixel edges to speed-up charge collection.

In both cases the reverse biasing of the sensing node is obtained through the front side, by applying a positive potential directly to the collection electrode and keeping the substrate grounded. For each front-end architecture the implementation is slightly different and a more detailed description is presented in Section 2.2.

2.1. Pixel matrix

A high level functional block diagram of the CE-65 chip is shown in Fig. 1. The chip is built of several major blocks: the pixel matrix, column and row selectors, column buffers and the output buffer. For the two variants reported in this paper the matrix size is 64 × 32 pixels.

The matrix is read out in rolling shutter mode with a configurable integration time down to 50 µs, translating to readout speed up to 40 MHz, although the presented results have been obtained with the read-out clock frequency lowered to 10 MHz. The signal is digitized outside the chip by a fast 16-bit Analogue-to-Digital Converter, defining the signal arbitrary digital unit (ADU).

2.2. Pixel architecture

The pixel matrix is divided into three sub-matrices that incorporate different in-pixel electronics architectures. Different readout flavours have been implemented: both a source follower with gain below one, and an amplifier with gain of about five have been used, both in a version where the sensor is DC coupled to the readout input, and in an AC coupled version inserting a custom metal to metal capacitor (C_{SEP}).

The AC-AMP and DC-AMP in-pixel circuitry is shown on the left side in Fig. 2. In the AC-AMP, the sensing node (reversely biased diode to substrate) is DC separated from the input stage of the readout electronics by the capacitance C_{SEP} (~10 fF). This AC coupling allows to be more flexible in the reverse biasing of the sensor, as the readout circuit is not exposed to the DC component of the sensor bias. Thus, the voltage applied to the resetting diode (*HV_RESET*) is not limited by the electronics supply voltage. The second sub-matrix DC-AMP exploits the same in-pixel electronics, with the pre-amplifier followed by a level shifter. The sensing node is directly connected to the gate of input transistor. Thus, the reset diode is no longer present and the input node voltage is determined by the pre-amplifier operating point. In the third approach shown on the right side in Fig. 2 a simple 3T-like source follower architecture has been utilized. The reset diode has been implemented similarly as for AC-AMP, but the reset voltage is directly transferred to the gate of the input stage, so *VRESET* cannot exceed the supply limits.

3. Analysis results

The initial laboratory tests presented here are focused on comparing the basic and optimized diode performance. Measurements have been done with ^{55}Fe radioactive source at room temperature. The substrate back bias voltage was set to 0 V.

Data samples have been processed so that the final signal value of each pixel is extracted from the difference between its raw amplitudes in two consecutive frames. Hits from impinging particles are identified from seed pixels with a signal over noise ratio larger than 10. Then clusters are built from the set of 3 × 3 pixels surrounding seed pixels.

3.1. Baseline and noise

The baseline and Equivalent Noise Charge (ENC) performance for both basic and optimized diodes are showing no significant differences as expected from the design, thus Fig. 3 presents results only for the basic structure. The baseline map reveals clearly the sub-structure corresponding to different in-pixel circuits. However, among the submatrix, the baseline is uniform, showing only small degradation towards the edges. ENC was calibrated based on the ^{55}Fe spectrum (see next subsection) and no significant differences are observed between submatrices. Preliminary results show that the noise performance depends on the settings optimization and biasing condition, but in most of the cases the measured ENC values are within the range of 15 to 25 e^-.

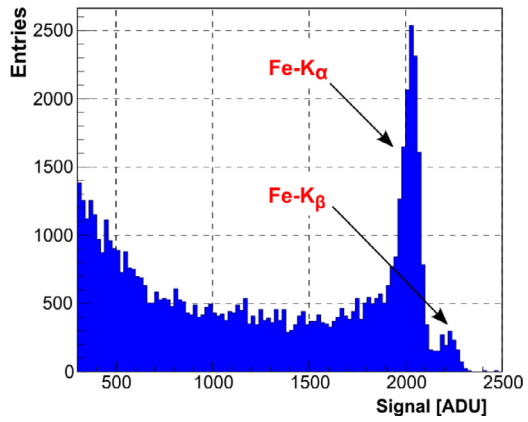

Fig. 4. Iron source spectrum of single pixel clusters from one source follower pixel — optimized diode.

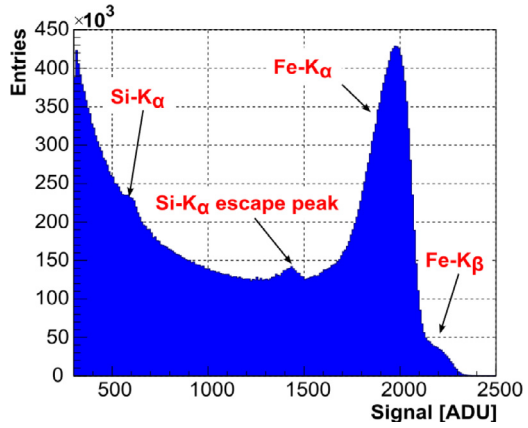

Fig. 5. Iron source spectrum of single pixel clusters from whole DC-SF submatrix for optimized diode.

3.2. ^{55}Fe energy spectrum

The ^{55}Fe energy spectrum is obtained from single pixel clusters, where the seed pixel carries almost whole cluster energy. The spectra are shown for the DC-SF submatrix with optimized diode, but results obtained with other in-pixel circuitries are very similar.

Fig. 4 shows the ^{55}Fe spectrum for one pixel selected from the SF-matrix. This approach allows to get rid of the pixel-to-pixel gain variation at the cost of reduced statistics. A clear separation between the two characteristic lines Fe-K$_\alpha$ (5.90 keV) and Fe-K$_\beta$ (6.49 keV) is observed and confirms the low pixel noise as well as a promising energy resolution.

In Fig. 5, the single pixel cluster spectrum is presented for the whole DC-SF submatrix. The peaks are clearly smeared by the pixel-to-pixel variations, but still both Fe-K$_\alpha$ and Fe-K$_\beta$ lines are distinguishable. However, the larger statistics reveals two additional energy lines: the Si-K$_\alpha$ (1.74 keV) and silicon escape peak (4.16 keV). The peak positions obtained from Fig. 5 allows the extraction of the detector energy calibration curve, depicted in Fig. 6. A high linearity is observed with an intercept close to zero.

3.3. Charge collection and sharing

Including all clusters in the ^{55}Fe data analysis allows additional observations. The comparison of the spectra obtained with the basic and optimized diode geometries from the AC-AMP pixels with a bias voltage of 10 V, are shown in Fig. 7, where the signal carried by the seed pixel only and the total cluster signal are plotted respectively.

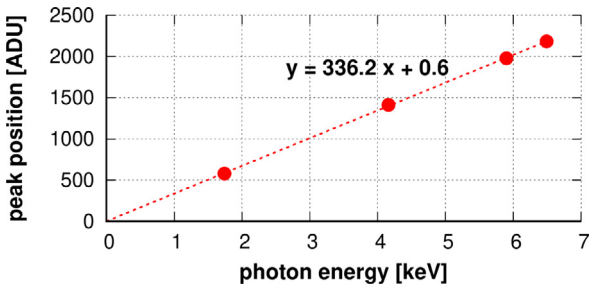

Fig. 6. Calibration curve of photon energy to ADU for DC-SF optimized diode, superimposed with a linear fit (dashed line).

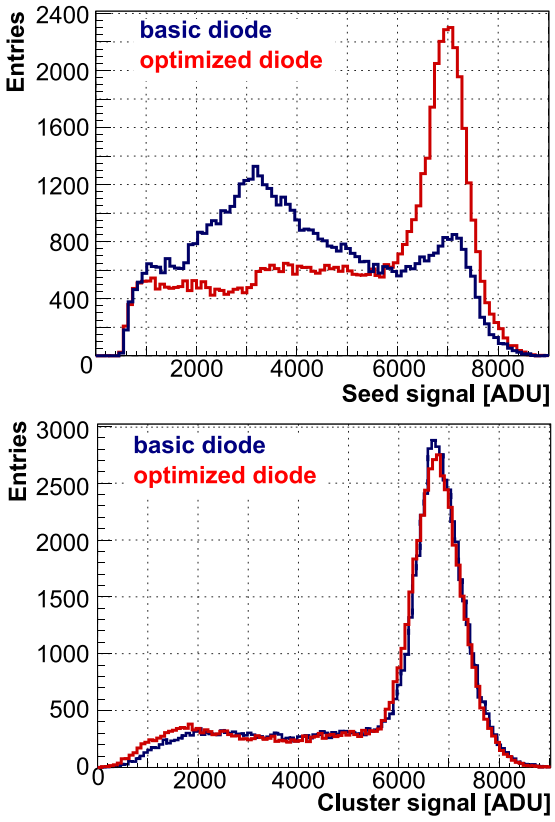

Fig. 7. Basic (blue) and optimized (red) diode comparison: signal contribution from seed pixel (top) and total cluster signal (bottom).

For both collection nodes, the Si-K$_\alpha$ peak is easily visible at the end of the seed pixel signal distribution, corresponding to single pixel clusters. The total cluster signal is almost located at the Si-K$_\alpha$ position in ADU in both cases, indicating that the two diodes feature an excellent charge collection efficiency.

However, the seed pixel signal distributions show divergent features. For the optimized diode, both the cluster and seed pixel spectra look very similar with a single peak at the Si-K$_\alpha$ line location, indicating that the vast majority of the total charge is systematically collected by the seed pixel. In contrast, for the basic diode the seed pixel spectra features an additional broad peak with slightly less than half the total cluster signal. This is a strong sign that a significant fraction of the signal charge is shared with neighbouring pixels.

A more quantitative comparison of the charge sharing between basic and optimized sensor diodes is provided by the maps of the average pixel contribution to the total cluster signal, as presented in Fig. 8. The significant charge sharing for the basic diode structure is confirmed, since the seed pixel collects in average slightly less than half of the total

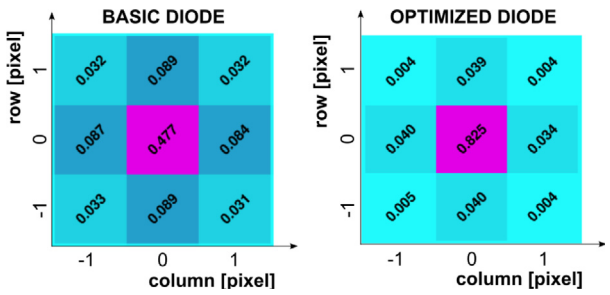

Fig. 8. Average contribution to cluster signal for individual pixel in 3 ×3 clusters.

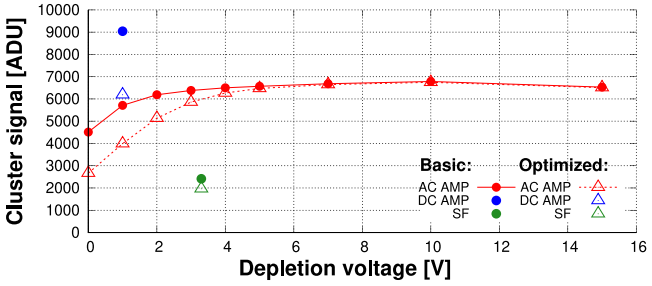

Fig. 9. Evolution of Fe-K_α peak signal amplitude in function of the reverse bias voltage across the sensing node for the various CE-65 pixel structures.

cluster signal. The electric field in the optimized diode is designed to accelerate the charge from the pixel edge to the collection electrode, and strongly suppresses charge sharing.

3.4. Depletion studies

Depletion of the sensor volume can be achieved by applying negative back bias voltage to the substrate or utilizing AC coupling and directly biasing the collection node. Since applying substrate potential other than ground causes a significant shift of electronics operating points and affects the detector performance, for the study of the depletion development in the sensitive layer, only the second biasing method was exploited.

The Fe-K_α peak position with respect to the applied biasing voltage (for all investigated cases) is shown in Fig. 9. Focusing on the results for AC-AMP, one observes that for both diodes geometries depletion develops up to about 5 V and afterwards saturation is reached.

While at higher reverse biases the signal amplitude is comparable for the standard and optimized sensor, at lower biases the amplitude degenerates faster for the optimized sensor due to a faster increase of the sensor capacitance. Marginal conclusions could be made for submatrices DC-AMP and DC-SF, for which the biasing voltage is fixed by design. One could however notice, that the ratios between optimized and basic structures are preserved, as expected. The differences in gain between submatrices are also in agreement with the simulations, showing that DC-AMP have about 5 times higher gain than DC-SF while for the AC versions it is only 3 times higher (due to parasitics introduced by the separation capacitance).

4. Conclusions

This work presented the initial performance studies of the CE-65 monolithic CMOS sensors fabricated in the 65 nm TPSCo process, during the first submission organized by CERN to explore this technology. The tested CE-65 variants, with a 15 µm pixel pitch, showed low noise operation and uniform pixel baseline among submatrices. Excellent charge collection efficiency was obtained in measurements. While significant charge sharing has been measured with a basic collecting diode, an optimized structured was demonstrated to strongly mitigate this effect. As a consequence, the basic diode might be more appropriate for applications targeting outstanding spatial resolution. On the other hand, charges are more focused on a single collection node for the optimized structure, which is beneficial for the time resolution and tolerance against radiation generating bulk damage.

Complementary results characterizing CE-65 will come from irradiated samples and on-going test-beam analyses. In addition, further studies will be conducted with the next submission of CE-65 prototypes.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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