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5 **A 64-channel waveform sampling ASIC for SiPM in** 6 **space-born applications**

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12 **ABSTRACT:** The architecture of a 64-channel ASIC for the readout of Silicon Photomultipliers in
13 space experiments is described. Each channel embeds a front-end amplifier with a common gate
14 topology followed by a 256 cells analogue memory with a sampling frequency of 200 MHz. A
15 single memory cell includes a storage capacitor, a single-slope Analog-to-Digital Converter (ADC)
16 with programmable resolution between 7 and 12 bits and the digital control logic. To save power,
17 the A/D conversion is carried-out only when a trigger signal is received. The trigger can either be
18 generated inside the ASIC or provided by an external source. The analogue samples are digitized in
19 parallel, thus reducing the conversion dead time. The memory cells can be arranged in a single array
20 or they can be grouped in shorter slots of 32 or 64 cells that work in a multi-buffer configuration.
21 The channels can work independently or they can be synchronised to acquire the same time-frame
22 in the full chip. The target power consumption is 5 mW/channel. The ASIC is being designed in a
23 65-nm CMOS technology. A digital-on-top flow is applied for the integration and final validation
24 of the chip. The tape-out is scheduled in the first quarter of 2023.

25 **KEYWORDS:** VLSI circuits, Front-end electronics for detector readout

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32 **1 Introduction**

33 Silicon Photomultipliers (SiPMs) are today employed in many different fields such as High Energy
34 Physics (HEP) instrumentation [1], LIDAR [2], Positron Emission Tomography (PET)[3]. Due to
35 their good detection efficiency, compactness and capability to work with moderate power supply
36 voltages they are becoming more and more attractive also for space-born applications. SiPM are
37 considered, for instance, to equip on board cameras of future satellite-based cosmic ray observato-
38 ries. In this context, they will be used to detect the Cherenkov light produced by the interaction of
39 Ultra-High Energy Cosmic Rays (UHECRs) and neutrinos with the terrestrial atmosphere [5].

40 Two common approaches to readout SiPMs rely on charge integration [6] or photon counting
41 technique [7]. However, these solutions do not allow to study in detail the signal waveform and,
42 as a consequence, to distinguish the signal of interest from spurious signals created by the direct
43 interaction of cosmic rays within the sensor. For the method to be effective, the waveform should
44 be captured with a sampling frequency of at least 100 Ms/s. A large dynamic range (up to 12 bits)
45 is also required as the energy of the primary particle can span several orders of magnitudes. High
46 integration density is desired to keep the overall system compact and lightweight and low power
47 dissipation is mandatory. Therefore, a single channel should offer a complete signal processing
48 chain with a power budget of only a few milliwatts. Care must be paid to radiation tolerance as
49 well, with particular emphasis on Single Event Effects. On the basis of these considerations, the
50 design of a custom ASIC optimized to read-out a SiPM-based Cherenkov radiation imager has been
51 undertaken. The key target specifications are a sampling frequency of 200 Ms/s, a maximum power
52 consumption of 5 mW/channel and a dynamic range of 12 bits.

53 **2 ASIC architecture**

54 The 64-channel ASIC is being designed in a commercial 65-nm CMOS technology and must operate
55 with a power supply of 1.2 V. The choice of the technology stems from the fact that it provides a good
56 integration density and its radiation tolerance has been extensively studied. The straightforward
57 approach in a waveform sampling system, is having one free running ADC per channel followed by
58 a digital signal processor. Despite the impressive progress made in ADC developments [8], [9], the

59 use of one 12-bit ADC per channel would hardly be compatible with the target power consumption.
 60 Furthermore, since the flux of UHECRs is extremely low (0.1 to 100 particles per hour are expected
 61 [10]), a continuous digitization is unnecessary. Analog memories provide instead an interesting
 62 alternative to capture fast transient signals occurring sparsely in time.

63 The block diagram of one channel is shown in figure 1. The current pulse coming from the
 64 sensor is amplified and converted into a voltage by the input amplifier. The resulting voltage is
 65 buffered into a 256-cells analog memory which is used to store temporarily the signal information.

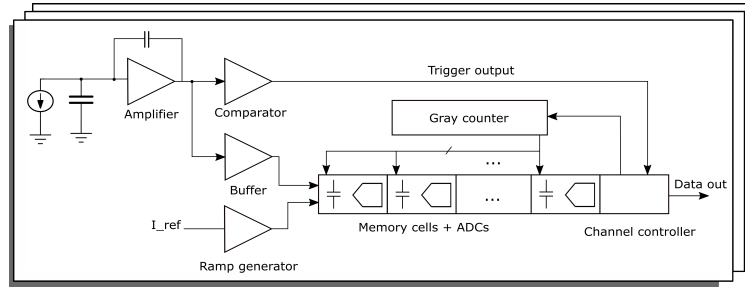


Figure 1: Channel block diagram.

66 When the sampling is enabled, the cells are written with a frequency of 200 MHz and the
 67 memory works as a ring buffer. If an event occurs, a trigger signal is issued and the cells enter the
 68 digitization phase, otherwise they are overwritten. In order to perform background monitoring, an
 69 external trigger can be sent to the chip. The analog memory can work as a single buffer or it can
 70 be divided into a maximum of 8 segments of 32 cells each thus enabling multi-buffering mode. By
 71 segmenting the analog memory, the data are derandomized, so the system can acquire an event even
 72 if the processing of the previous one is still in progress. Furthermore, the channels of the ASIC can
 73 be programmed to operate in parallel (imaging mode) or independently from each others (sparse
 74 mode). The digitized data are transmitted off-chip by employing a 8-channel Double Data Rate
 75 (DDR) serializer operating with a frequency of 400 MHz.

76 2.1 Front-End

77 The front-end amplifier is based on the common gate topology [11]. Both polarities of the amplifier
 78 have been implemented to read positive and negative pulses thus increasing the flexibility of the
 79 chip. The two schematics are shown in figures 2a and 2b. This stage includes also a comparator
 80 to provide a local trigger. In sparse mode, each channel is triggered independently. In imaging
 81 mode, two trigger modalities are foreseen: a fast or between the channels and a topological trigger
 82 that looks at the firing on nearby channels. The generated information can either be used to trigger
 83 a readout sequence directly on the chip or it can be provided as primitive to an external trigger
 84 processor, that looks at the trigger outputs of different ASICs before issuing a final trigger decision.

85 2.2 Analog Memory

86 The basic building blocks of the analogue memory is the sampling cell. Several options can be
 87 considered to digitize the sampled data. One possibility is to have a fast ADC per channel or
 88 per group of channels. However, even using a moderate speed ADC (e.g. 20 Ms/s), 12.8 μ s are

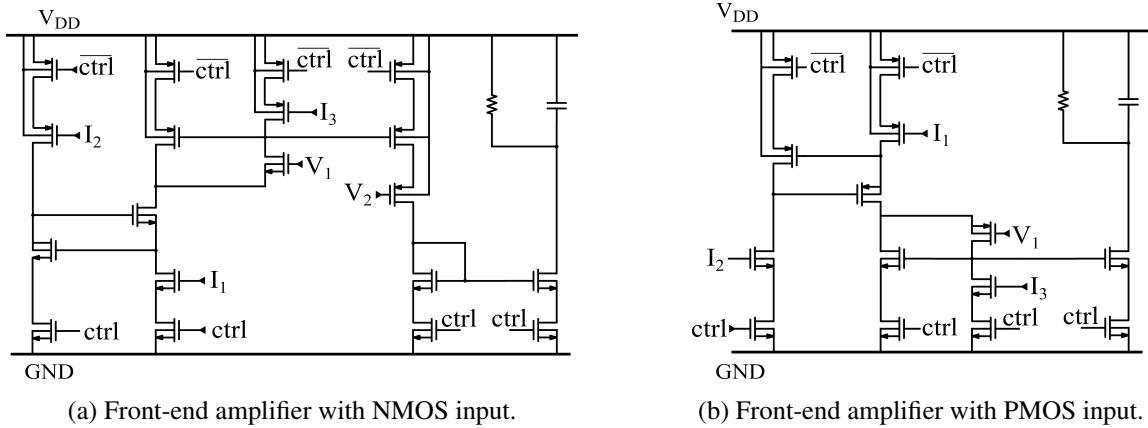


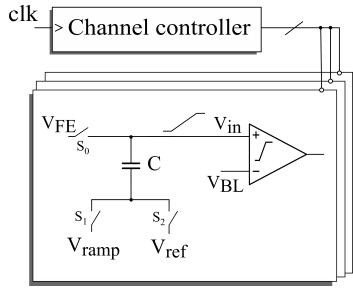
Figure 2

89 needed to readout 256 cells. The Wilkinson ADC topology is attractive for its simplicity, but it has
 90 long conversion time. However, it requires a limited number of hardware resources. Therefore, a
 91 massive parallelism can be used to keep the overall conversion time of the memory to an acceptable
 92 level. For instance, in [12] a fast sampling ASIC with an analog memory of 128 cells is described.
 93 The digitization is fulfilled by using 128 10-bit single-slope ADCs placed at the periphery of the
 94 chip. Therefore, all the cells in a single channel are converted in parallel. However, the scaling
 95 in CMOS technologies allows to develop chip with even higher integration density. Hence, in our
 96 device a 12-bit single-slope ADC has been embedded directly in each memory cell. This allows to
 97 digitize all the samples in the ASIC in parallel thus reducing the dead time. The time needed for
 98 the conversion is given:

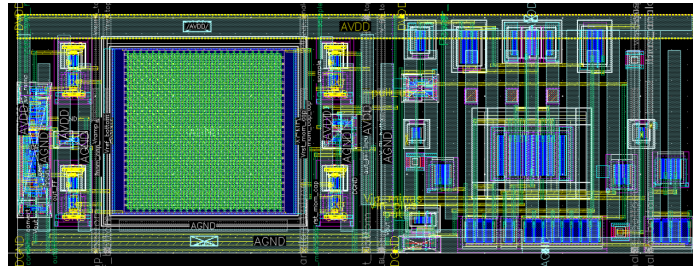
$$2^N \times T_{clk} = 20.48 \mu m \quad (2.1)$$

99 where N is the resolution and T_{clk} represents the clock period of 5 ns. The resolution of
 100 the converter can be programmed between 8 and 12 bits. Hence, with a lower resolution, this
 101 time interval is decreased. For instance, for a 10-bit resolution (that could still adequate for our
 102 purpose) the conversion shrinks to $5.12 \mu s$. However, in a waveform sampling ASIC an important
 103 contribution to dead time is also given by data transmission. In fact, the digital data stream is
 104 composed of a 27-bit long header and the digitized data. By selecting the maximum resolution
 105 for the ADC, an amount of 3099 bits per channel must be transmitted to readout 256 cells. Even
 106 using 10 Gbit/s serializer per chip the time to send the raw data out would be $19.83 \mu s$. Data could
 107 be of course zero-suppressed and compressed on chip before transmission. However, it has been
 108 preferred to defer a more elaborated signal processing to the on-board FPGA. To increase the system
 109 modularity and thus its fault tolerance, instead of using a single, fast serializer 8 DDR serializers
 110 working with a 400 MHz clock have been implemented. This allows to segment the ASIC in
 111 modules of 8 channels which are basically independent of each other. The data transmission time
 112 thus becomes $30.99 \mu s$ in the worst case in which all the 256 cells are used to capture a single event.

113 The building blocks of the memory cell are shown in figure 3a. Each cell includes the sampling
 114 capacitor, the comparator of the ADC, some switches and a control logic (not illustrated in the
 115 figure). A single Gray counter whose outputs are shared among the ADCs, is embedded in each



(a) Memory cell building blocks.



(b) Layout of the memory cell.

Figure 3

116 channel. In the sampling phase, the storage capacitor is charged to a voltage equal to $V_{FE} - V_{ref}$,
 117 where V_{FE} is the output of the input amplifier and V_{ref} is a reference voltage. In contrast with the
 118 most common architecture [13], the minus terminal of the comparator is not connected to a ramp
 119 generator. In fact, this solution can deteriorate the linearity of the system because the common mode
 120 of the comparators changes between the cells. A possible solution consists in fixing the threshold
 121 to a steady value while charging the capacitor through a constant current generator. However, the
 122 mismatch between the current sources can lead to gain variation between the cells. Hence, a single
 123 ramp generator is applied to all the storage capacitor. During the digitization the top plate of the
 124 capacitor is connected only to a gate terminal of a MOS transistor, so this node remains floating.
 125 Hence, if a ramp generator is connected to the bottom plate, the same voltage variation is replicated
 126 on the top thanks to charge conservation. When the voltage on this terminal reaches the threshold,
 127 the comparator flips triggering the storage into local latches of the output of the Gray counter. This
 128 allows to embed a single ramp generator which is common to all the cells in a single channel as
 129 shown in ref. [13], but this alternative approach ensures good gain uniformity between the cells.

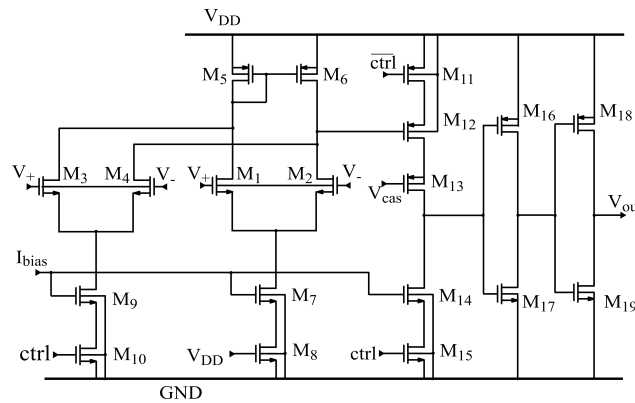


Figure 4: Comparator schematic.

130 The schematic of the comparator is shown in figure 4. It has two possible states which are
 131 called power-up and power-down mode. In power-up mode, a bias current of $2 \mu A$ is provided to
 132 this block. On the other hand, when the digitization is disabled, the current is reduced by three
 133 quarter in order to reduce the power wasting when the comparator is not operating. However, this

134 block is not completely switched off thus allowing a fast warm-up. Hence, before digitization, 1-2
135 clock cycles are dedicated to power up of the converters and to switch the bottom plates of the
136 capacitors from the fixed reference to the voltage ramp.

137 The final layout of the cell has a size of $43.62 \times 15.20 \mu\text{m}^2$ and it is illustrated in figure 3b.
138 This sizing allows to integrate the analog memory in a chip with final dimensions of $6\text{mm} \times 4\text{mm}$.

139 The analog cell is integrated with a digital-on-top methodology. Figure 5 reports a preliminary
140 layout where the Wilkinson ADC is included alongside the latches. The upper part of the image
141 depicts the layout of block named section in which the cells are hierarchically organized and the
142 ensemble of the eight sections. Each section is managed by a digital channel controller (not shown
143 in the layout) where dedicated Finite State Machines (FSMs) are implemented. These FSMs take
144 into account the partitioning of cell array by appropriately managing the sampling, digitizing and
145 readout states. The channel controller also drives the configurable Gray counter whose output is
146 distributed to each section. A first estimate of the digital power was evaluated by synthesizing each
147 block and the consumption is limited to 1.3 mW per channel. Since this value does not consider
148 the final routing, a variation around 30 % is typically expected.

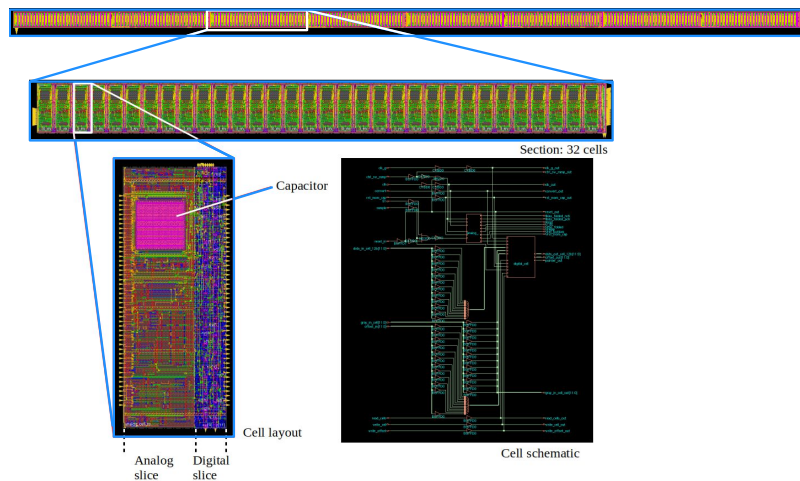


Figure 5: Layout of a section

149 3 Conclusions

150 This paper presented the architecture of a 64-channel ASIC for SiPM readout in space environment.
151 The input current pulse is amplified, converted into a voltage value and stored into a 256-cells analog
152 memory. The memory cells allow to acquire a snapshot of the incoming event with a resolution
153 of 12 bits. Sampling and digitization steps are decoupled since the conversion starts only if a
154 trigger signal (both generated internally or provided from the outside) is received. This allows to
155 obtain lower power consumption compared to the implementation of a free-running converter. The
156 chip flexibility has been increased by applying the derandomization technique. The ASIC is being
157 designed in a commercial 65-nm CMOS technology. The power consumption aims to be 5 mW/ch
158 considering both analog and digital circuits. The integration of the building blocks is ongoing and
159 the chip tape-out is scheduled at the beginning of 2023.

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