Pixel Read-Out Architectures for the NA62 GigaTracker.

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Abstract

Beam particles in NA62 experiment are measured with a Si-pixel sensor having a size of 300 µm x 300 µm and a time resolution of 150 ps (rms). To meet the timing requirement an adequate strategy to compensate the discriminator time-walk must be implemented and an R&D effort investigating two different options is ongoing. In this presentation we describe the two different approaches. One is based on the use of a constant-fraction discriminator followed by an on-pixel TDC. The other one is based on the use of a Time-over-Threshold circuit followed by a TDC shared by a group of pixels.

The global architectures of both the front-end ASIC will be discussed.

I. THE GIGATRACKER SYSTEM

The aim of the proposed NA62 experiment at the CERN SPS is to study the very rare decay of the charged K meson into a pion and neutrino-antineutrino pair. One of the key components of NA62 will be the GigaTracker, which consists of three matrices of Si-pixel stations, each covering a sensitive area of 60 mm x 27 mm. Each pixel is 300 µm x 300 µm [1].

The GigaTracker is designed to measure the beam particle trajectory with a space resolution of 100 µm (rms) and a timing accuracy of 150 ps (rms). In order to reconstruct the momentum of the beam particles a system of four dipoles, A1…A4 in Fig.1, provides the momentum selection followed by the beam recombination.

The timing resolution of 150 ps (rms) is an unusual requirement for a traditional pixel detector and none of the existing systems has such a capability. Other challenging aspects are due to the high radiation operational environment and the very low material budget restraint (0.5% X_0 per station, sensor thickness 200 µm, read-out chip thickness 150 µm).

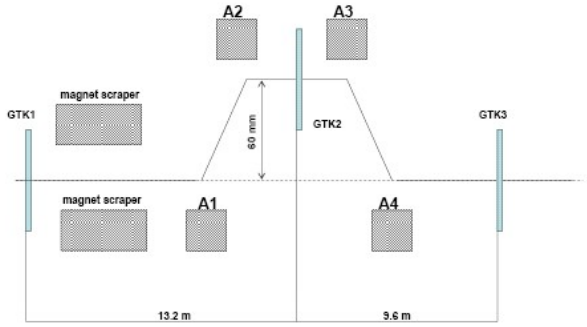

Figure 1: GigaTracker system

Each silicon sensor will be read-out by 10 front-end ASICs, with 45x40 read-out cells each.

The 10 read-out chips will be bump-bonded to the pixels, so only one side of the chip will be used for external connections (wire bonding pads in Fig. 2).

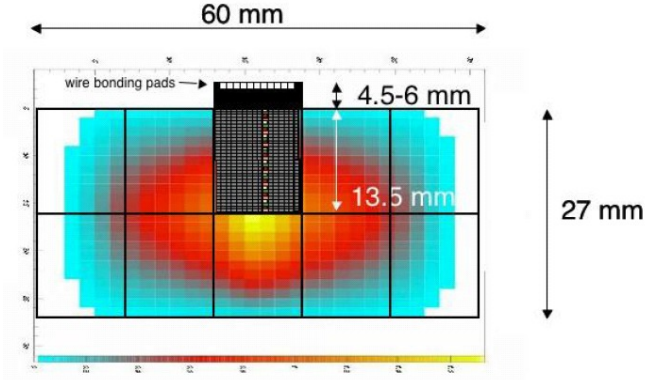

Figure 2: Sensor and read-out chips

The particle rate, which is higher in the central part of the sensor, is estimated to be ~1.5 MHz/mm^2 maximum, which corresponds to 130 MHz per chip and 140 kHz per

pixel and almost 1 GHz over the whole system (thus the name GigaTracker) [2].

In order to partly recover the radiations effects (10^5 Gy of total dose is expected in one year) the system will be cooled at 5^o C or less and it will be replaced after a runtime of 60 days of work under optimum beam conditions.

II. READ-OUT CHIP OVERVIEW

The total average data rate per chip it will be around ~4.2 Gb/s, which corresponds to a maximum of ~6 Gb/s with fluctuations. Due to the huge amount of data to transfer, high speed serial links will be adopted and a trigger less read-out solution will reduce the amount of data to store inside the chip itself. In addiction the read-out chip should achieve the efficiency of 99%.

Two major issues have to be addressed to achieve the required time resolution: the compensation of the discriminator time-walk and the time measurement with such a high density of channels.

Time-walk problem can be addressed either via a Constant Fraction Discriminator (CFD) or a Time-Over-Threshold (TOT) correction. While the first approach requires only one measurement per hit, it poses more challenges on the design of the comparator.

The coarse time information will be provided by a clock counter. The issue of precise time resolution with a high read-out channel density can be dealt either with a Time-to-Amplitude Converter based TDC serving a single pixel or via a bank of DLL-based TDC shared among several pixels.

The TAC-based TDC solution requires more circuitry on the pixel area, thus potentially creating noise problems. Moreover, the pixel area receives a high radiation dose and therefore it has to be designed in order to be radiation-tolerant in both total dose and SEU aspects.

On the other hand, the DLL-based TDC has to be much faster in order to keep the dead time under control because the TDC is shared among pixels. Ambiguities can arise if two pixels which belong to the same TDC are hit close in time. Moreover, the TDC bank has to be placed at the end of the pixel column and therefore the signal carrying the time information has to be transmitted over a well calibrated transmission line in order not to degrade the timing information.

Preliminary investigations did not give a clear advantage of one solution over the other, therefore two prototypes will be designed in order to have an experimental comparison of the performances. For both architectures a demonstrator chip will be soon submitted in CMOS 130 nm technology.

III. ON PIXEL TDC ARCHITECTURE

This architecture will perform the walk time compensation by a Constant Fraction Discriminator filter (CFD) and the TDC option is a Time to Amplitude Converter (TAC) based on a Wilkinson ADC. Both CFD and TDC are implemented on the pixels cell, as shown in Fig. 3.

The preamplifier is bonded to the sensor and its output processed by the CFD filter. When a hit is detected the content of the coarse bus (coarse time information) is latched into a digital buffer. In parallel the hit triggers a ramp generator to charge a capacitor. The charging up is terminated by the semi-clock trailing edge. The voltage is then converted in the fine time information by the Wilkinson ADC. The whole information (coarse time, fine time and pixel address) is stored into the output buffer before being transferred to the end-of-column logic.

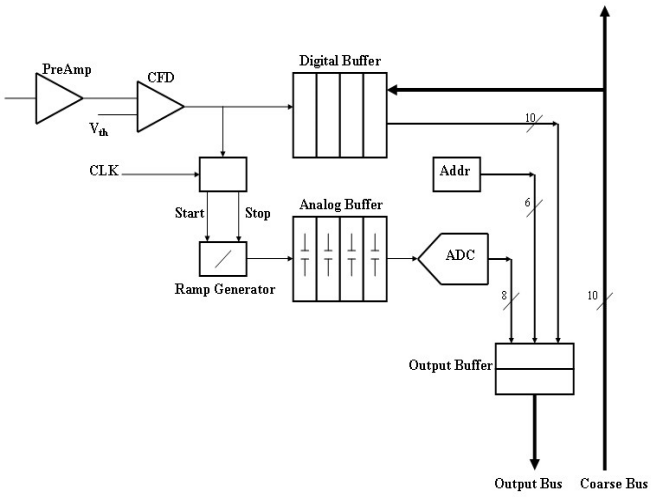

Figure 3: The pixel cell model for the on pixel TDC architecture

The system clock frequency is 160 MHz; the coarse time is measured with 10 bits, while the fine time occupies 8 bits. Finally the TDC binning is ~98 ps. One of the advantages of this architecture is the derandomization performed directly on the pixel cell and the very low dead time which is only due to the ramp generator or in case of buffers overflow. Exhaustive simulations have been performed in order to evaluate the FIFO depths (4 for the inner ones, 2 for the output one) and the number of lost events due the dead time (< 0.2% at 140 kHz).

The whole read-out chip is organized in column of 45 pixels each. The Column Controller performs the data reading and formatting. Then a group of m columns (where m it depends on the output speed) is connected through the Matrix Controller and merged before to be read-out by a high speed serial output.

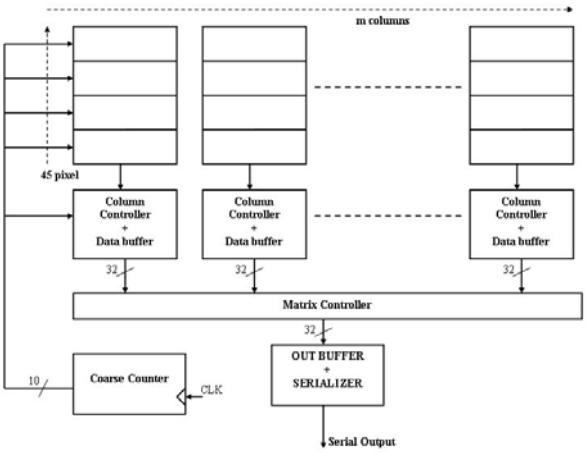

Figure 4: Read-Out chip overview

A first prototype of this read-out chip is going to be submitted by the middle of November 2008, using the IBM CMOS8RF technology (130 nm). The chip is made of 3 columns of pixels cells, fully equipped as described before.

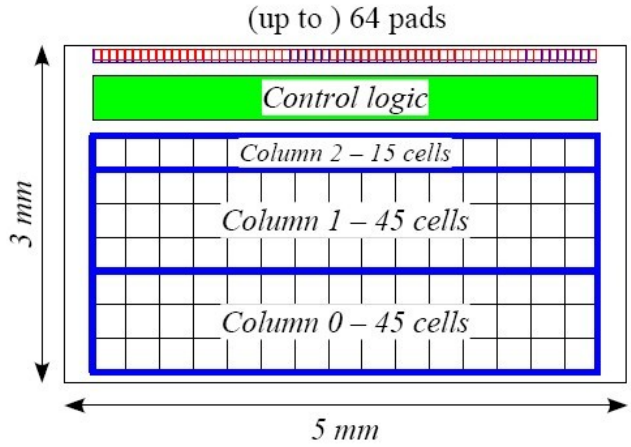

Figure 5: demonstrator chip's layout overview

Two columns have all the 45 pixels and they are folded as shown in Fig. 5. Another column of only 15 pixels is added in order to study corners effects in case of problems with the folded columns. The Control Logic area is hosted in the 3 Column Controller, the coarse counter and the I/O drivers.

IV. End of Column TDC architecture

The basic principle of the End Of Column (EOC) architecture is simple, but the implementation is challenging. Essentially, it consists of performing only the essential analogue signal processing functions in the pixel cell. The signals from the sensors are sent to a preamplifier and then to a Time Over Threshold discriminator. The ToT output fast hit signals are transmitted with constant amplitude and pulse width proportional to the input charge to the EOC circuits using transmission lines operating at low signal level in current mode. With this technique the pulse width information is used to correct offline for the time walk. All the rest of the processing functions, as hit time stamping, pixel address encoding, data pipelining in FIFO, and data formatting are done in the far end EOC on the chip periphery.

Each column is organized into two separate bus systems. The first is the data bus which transmits the hit information, leading edge and trailing edge. It comprises 9 coplanar transmission lines, where each line is connected to 5 pixels. The other 5-bit bus contains the address of 9 pixels. The EOC logic matches the signals from the two buses and determines in a unique way the hit address. This bus architecture is a compromise between the huge data flow, each 45-pixel column has peak occupancy of 4 M hits/s and an affordable number of lines of the column bus. The column bus transmits hit information to TDCs placed at the end-of-column. To maintain the efficiency higher than 99%, the solution used in the readout is to keep the column segmentation up to the serializer, as shown in Fig.6, and then connect each column output port to an on-chip or off-chip multiport parallel-in-serial-out Gigabit serializer. Finally the serializer drives the optical fibre Gigabit link. At the end of column, the architecture logic works both in pipeline memories and to equalize data rate fluctuations maximizing the throughput rate.

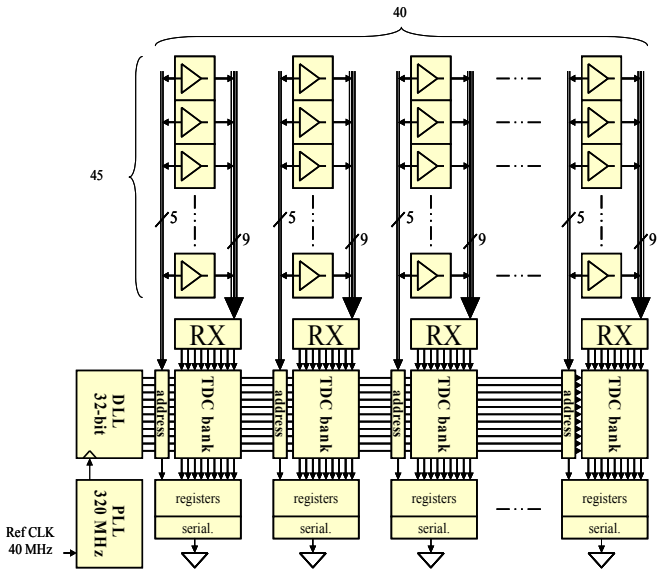

Figure 6: EOC architecture

The TDC bank contains 9 TDC (each one serves 5 different pixels). Each of them contains 2 hit registers (leading edge and trailing edge) 32 bit each.

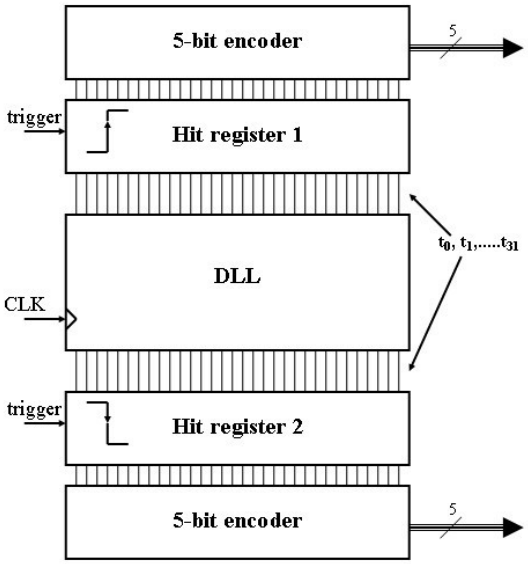

Figure 7: TDC architecture

The DLL based TDC consists of 32 delays elements, 100 ps each and it is driven by a reference clock of 320 MHz. The fine time information of 32 bits is then encoded in 5 bit words, in order to reduce the amount of data. In addiction the EOC also fit 2 more 6-bit counters, to give the coarse time information of the leading edge and the trailing edge. In total, when 5-bit encoders are not implemented, 81 bits of information per hit will be generated.

Also for this architecture a submission of a prototype is foreseen for the middle of November 2008, in IBM CMOS8RF technology (130 nm). It contains a whole folded column of 45 pixels, all of them equipped with the preamplifier and the TOT discriminator. In addiction a 15 pixels columns foreseen, in order to study effects of corners.

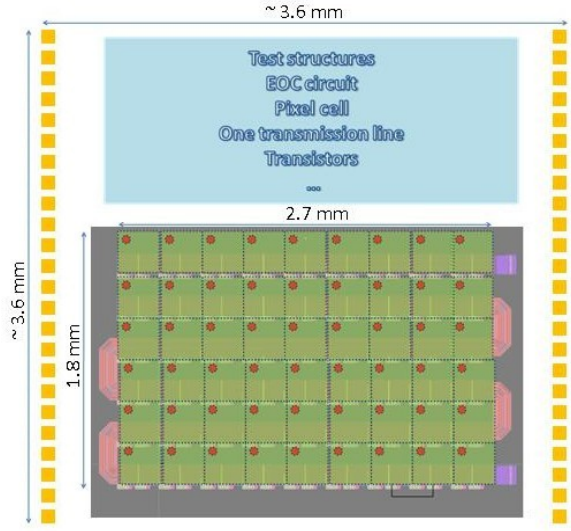

Figure 8: EOC demonstrator chip

Also the End of Column logic (TDC, Counters and data pipelining) will be implemented, for a total of 5+1 TDC. Data read-out is done by a serial LVDS driver.

V. SUMMARY

In Table 1 the main differences between the two possible read-out solutions are summarized. It's important to note that in one case (on pixel TDC) there is a major concentration of possible problems in the pixel cell (power, noise due the digital circuits, radiation effects) but it is expected to have better performances in terms of dead time and amount of data produced. The second option (EoC TDC) offers a simpler pixel cell (only analog circuits) but a more complicated system of analog transmission lines and a big concentration of digital sources at the end of column (TDC banks, hit registers, decoders and counters).

The two proposed architectures, for the GigaTracker read-out system, are quite balanced in terms of advantages and disadvantages, so there have been no a priori reasons, to adopt one solution over the other. Only the results of the two prototype chips can give an experimental verification of their performances.

Table 1: comparison between the two architectures

	On pixel TDC	EoC TDC
TDC option	TAC based 1 x pixel	DLL based 1 each 5 pixels
Time Walk Correction	CFD	ToT
On-pixel logic	Preamp+CFD+TDC+ data buffers	Preamp+ToT+line drivers
Signals to the EoC	Digital	Analog
Noise in the pixel cell	Higher due digital sources	Lower (only analog)
System CLK	160 MHz	320 MHz
Bits per hit	32	81
Dead time	Only during TAC ramp	Multiple hits on the same pixels group
Total dose and SEU issues	Digital logic on exposed area	Only analog circuits on exposed area
Power in the pixel cell	Higher	Lower
Power in the EoC area	Lower	Higher

VI. REFERENCES

[1] NA62 proposal (CERN-SPSC-2005-013 SPSC-P-326)

[2] The GigaTracker: Addendum to the NA62 proposal (NA62-07-08)