

Development of the ASICs for the NA62 pixel Gigatracker

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Abstract

We present the ASIC development for the readout electronics of the Gigatracker pixel detector of NA62. Specifications of this detector are challenging in terms of timing precision with a hit time stamp accuracy of 100 ps and a peak hit rate of 50 Mhits/cm²/s. A timing precision and hit rate are more than one order of magnitude faster than pixel LHC readout ASIC. The research for pixel cell design and the readout architectures are following two approaches, which are presented and discussed in this paper. Presently demonstrator prototypes are under development and SPICE simulation results of the frontend, the readout strategy and the pixel-column are also presented and discussed.

I. INTRODUCTION

The pixel Gigatracker system of the NA62 experiment consists of 3 stations with a surface of about 12 cm² each [1]. The pixel cell dimension is 300 μm x 300 μm. Specification are extremely challenging. The hit rates in the centre of the beam of 50 MHz/cm² and the timing precision of 100 ps results in a large output data rate of more than 4 Gbit/s/chip for the 1800 pixels of one chip. The radiation levels are expected to be 10⁵ Gy and the 1MeV neutron equivalent fluence is estimated to be 2 x 10¹⁴ cm⁻² each running year. In order not to degrade the momentum resolution a very low material budget of 0.45 % X₀ is targeted for. This small material budget imposes a pixel ASIC die thinned down to 100 μm and a thin silicon or diamond sensor of 150 to 200 μm thickness. It has a strong impact on the analogue front end sensitivity pushing discrimination threshold down to 0.5 fC. The timing precision of 100 ps imposes to use an ultra fast analogue frontend with signal peaking time in the range of 3-5 ns. There is no previous experience of such a challenging pixel system, and the NA62 collaboration has chosen two architectures to evaluate in the R&D phase. The two architectures are the pixel TDC architecture for which signal processing of hits are done in the pixel cell and the End of Column (EOC) architecture for which hit signals are sent to EOC peripheral circuits for processing.

The on-pixel TDC architecture pursues the classical pixel cell approach (i.e. in ALICE, ATLAS and CMS experiment) where the data processing is performed directly within the pixel cell. The pixel cell design is presented in section III.

The EOC architecture follows an approach for which the hit signals from the time-over-threshold discriminator of the analogue pixel cells are directly asynchronously transmitted to the End of Column (EOC). TDC circuits via transmission lines. This avoids the use of high speed clock in the active pixel array and allows an effective separation of the EOC CMOS digital signals from the analog frontend to minimize the digital crosstalk, already observed in current pixel detectors. The digital crosstalk is expected to be more severe with the fast discriminators used for the Gigatracker ASIC design.

Considering the high particle flux of the NA62 beam, strategies to enhance robustness against SEU are important for the on-pixel TDC option. The definition of the beam profile is such that outside the active area of 60 mm x 27 mm the particle flux is drastically reduced and thus electronics placed peripheral to the pixel matrix needs a reduced level of SEU protection. The EOC architecture option offers the advantage to substantially reduce the SEU risk, but poses the non-trivial challenge, to transmit high speed digital pulses up to 13.5 mm, while keeping timing precision to 100 ps without disturbing low noise preamplifiers in the pixel cells. The EOC architecture solution to this issue is presented and discussed in section IV.

II. SENSOR CHARACTERISTICS

The NA62 sensor baseline is a 200 μm thick pixelated p-in-n silicon sensor bumped to the ASIC. The active sensor size is 60 mm x 27 mm in order to fully cover the beam profile. The timing precision of 100 ps imposes a signal shaping of the electronic pixel channel of 5 ns peaking time. Such a fast shaping time puts a specific constraint to silicon sensor operation that should be close to saturation velocity. At carrier saturation velocity, the silicon sensor is expected to deliver full induced charge in approximately 4 ns as presented in Fig 1. However, such an intrinsic device speed might be not easily achievable in practice, and consequently there is a substantial risk of ballistic deficit [2].

After radiation sensor charge characteristics of the silicon sensor are degraded, and ballistic effect might severely affect signal to noise ratio of the electronic pixel channel.

One possible alternative of sensor that NA62 has considered is diamond [3].

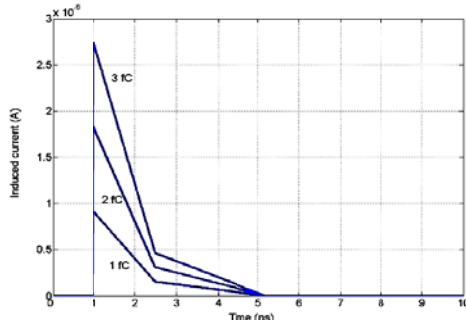


Figure 1 signal formation in silicon sensor operating at saturation velocity

Diamond has several advantages in terms of radiation length, carrier velocity, and radiation hardness. However, the charge delivered by one MIP is significantly smaller than in silicon at the same sensor thickness. A deeper study is mandatory to validate the use of diamond sensor.

III. NOISE ANALYSIS OF ANALOGUE PIXEL FRONT ENDS

The main design challenge of the analogue part of the pixel front end is extremely short 5 ns pulse peaking time, combined with minimising the power consumption, small Equivalent Noise Charge (ENC) and matching. Although the final version of the chip will contain trimming circuits, it is necessary to keep the mismatch of the threshold offsets at a reasonable level allowing a lower resolution of the trim DACs. Good matching together with satisfactory noise performance will permit lower threshold voltage improving timing performance of the comparator providing at the same time high efficiency of the detected signals and low noise occupancy. An analysis of the 130 nm CMOS8 RF LM/DM IBM technology is given in the plot Fig. 2, where ENC of the series, parallel and detector leakage noise contributions are expressed as a function of the total pixel capacitance in the case of an optimized preamplifier.

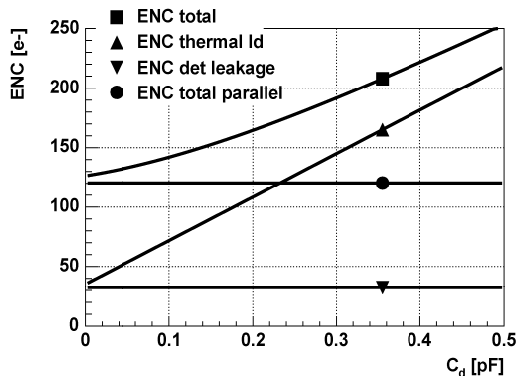


Figure 2 Noise characteristic of a preamplifier optimized for 5ns peaking time CR-RC3 and a pixel capacitance of 250fF. Input transistor bias is 40uA, feedback resistor 200kΩ, for detector leakage 20nA. At 200fF input capacitance, ENC is 170 e- rms with equal series and parallel noise contributions.

As one can see, for the 250fF detector capacitance we expect noise lower than 200e-. The actual gain of the front end amplifier is in the range of 70mV/fC and the simulated mismatch of the comparator offset is in the range of 6mV rms. (equivalent to 0.1 fC signal). Therefore the presented demonstrator chip will be able to operate with 0.7 fC threshold allowing both for very low noise occupancy, high efficiency and reasonable time walk of the comparator (1.5 ns

between 1 and 4 fC signal) further compensated off line with time-over-threshold measurement.

IV. ON-PIXEL TDC CELL

1) On-pixel TDC analogue pixel

The on-pixel TDC option has an architecture close to the traditional readout technique implemented in the ASIC of the LHC pixel detectors. Pixel cell comprises a preamplifier, shaper, discriminator time measurement and local buffering before transmission to the CMOS digital bus. However, the challenging requirements of the NA62 Gigatracker make circuit solutions adopted very different from LHC pixel design. The figure 2 presents the pixel analogue front end.

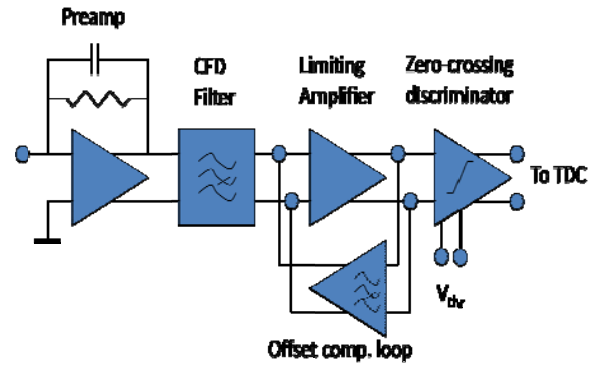


Figure 3 schematic diagram of the on-pixel cell

The preamplifier is optimized for a pixel capacitance of 250 fF, and it is followed by the Constant Fraction Discriminator (CFD) filter stage that performs the delay and subtraction with attenuated signal. Here the stage does not use a time variant filter as usually done for a CFD, but a continuous time filter that exhibits a close transfer function. Figure 4 shows SPICE simulation of the processed signals after the CFD stage.

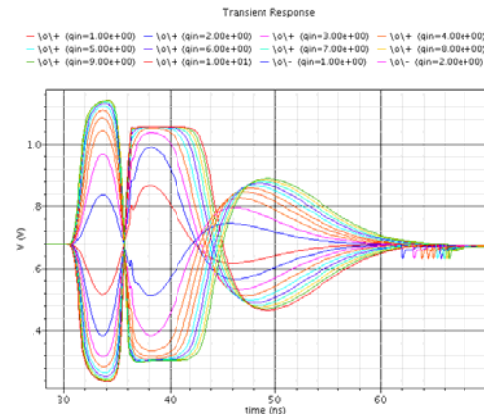


Figure 4 Signal shaping of the CFD stage for 1- 10 fC input charge

2) TDC based Time to digital converter

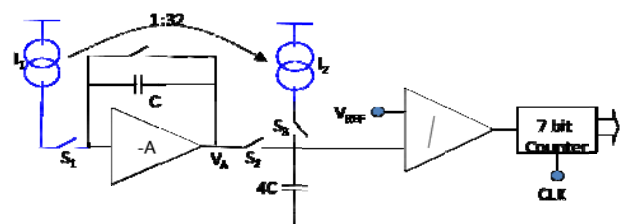


Figure 5 Schematic of the pixel TDC based on a Wilkinson time-to-digital-converter

The on-pixel TDC circuit is based on a time to analogue converter followed by a Wilkinson ADC. Figure 5 presents the pixel TDC. When a hit occurs, the leading edge signal generated by the CDF stage closes switch S1 and C is charged by I1. At the clock leading edge, S1 opens and a voltage proportional to the time interval is build up on C which is transferred to 4C when S2 closes. Then S2 opens and S3 closes which discharge linearly 4C to the V_{REF} potential. The generated ramp is then translated in a number of clock counts.

V. EOC PIXEL CELL

1) Pixel analogue front end

The pixel channel as presented in Figure 6 comprises 7 functional blocks:

- A transimpedance preamplifier
- A differential post amplifier
- A first stage of the discriminator
- Second stage of the discriminator with hysteresis
- A dynamic asynchronous latch comparator with transitional positive feedback
- A differential transmission line current driver with pre-emphasis
- A 300 μm length coplanar transmission line, not shown in the figure 6

The input stage is built around a cascode stage with an NFET input device biased at 40 μA and a feedback resistor of 200 $\text{k}\Omega$.

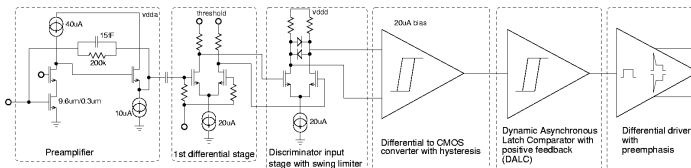


Figure 6 Block diagram of the pixel channel performing fast charge pre-amplification, hit discrimination, and driving transmission line in GHz bandwidth with current mode pre-emphasis. Bias current of the analogue pixel channel is 120 μA and 80 μA for the transmission line driver.

2) Bus based transmission lines

The EOC architecture entirely relies on the timing precision of low power signal transmission down to the end of column circuits. CMOS level signal transmission is excluded since it consumes too much power and generates too much digital noise in the active pixel array. A low swing current mode logic level has been adopted. The principle of the transmission line bus is presented in Figure 7.

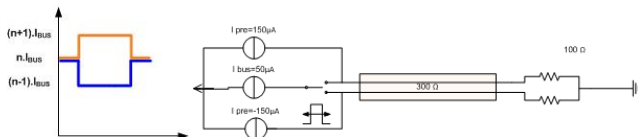


Figure 7 left: logic level +/- 50 μA on 250 μA bus bias current; right: lossy transmission lines driven with pre-emphasis

The bus system is based on lossy transmission lines integrated on the CMOS process [4,5].The bus architecture comprises for the data hit 9 transmission lines sharing 5 pixels distributed every 9 pixels to equalize pixel hit rate and for the pixel address 5 transmission lines sharing 9 contiguous pixels.

Each transmission line is driven in current mode and is the input resistance of receiver.

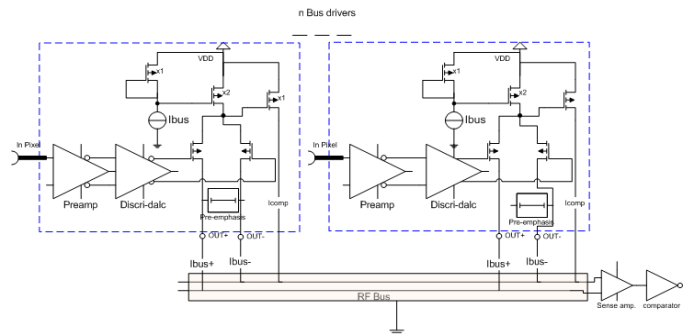


Figure 8 Schematic of the bus system based on transmission lines

The current driving is done by a differential switch that flips a current source when a hit is present. A second DC current source equalizes the DC current during steady state time. The current signal swing defining the logic level in coplanar waveguides¹ has been specified to $\pm 50\mu\text{A}$, with a differential swing of 100 μA . The far end sensing voltage is 10 mV for a receiver input resistance of 100 Ω , about twice the odd² characteristic impedance of the transmission line. This choice results from a trade-off between receiver biasing, line characteristic impedance and power consumption. The series resistance of the line varies from 6 Ω for one pixel distance to 300 Ω for 45 pixels distance (13.5 mm), making the maximum drop voltage 3 times the far end sensing voltage. However, this effect does not disturb signal discrimination because the far end amplitude does not change with the pixel to receiver distance thanks to the current drive operation.

The high series resistance of lossy transmission line in CMOS process has a strong impact to the signal integrity of the bus. It considerably degrades signal edge in slowing down rise time signal to about 1.5 ns after 13.5 mm signal propagation. To circumvent this effect a current pre-emphasis [6,7,8] is implemented in the line driver. The signal pre-emphasis is done by injecting a fast current pulse on the edges of the hit pulses. Figure 9 shows the efficiency of the technique.

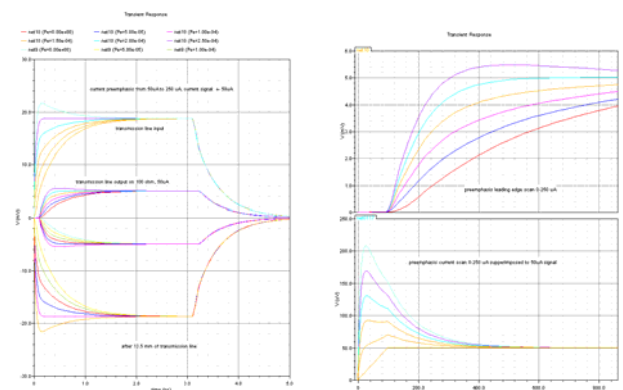


Figure 9 Current pre-emphasis, after 13.5 mm signal rise time is speed up by one order of magnitude from 1.5 ns down to 150 ps, for reference purpose in this simulation there is no pre-emphasis on trailing edge.

¹ The waveguide is a RF coplanar cross coupled transmission line design is specified and characterized by IBM.

² Cross coupled lines operates in anti-phase polarity and is characterized by the odd impedance.

3) End of column logic

The very low swing voltage imposes strong constraints on the sense amplifier design with the transmission line operating at a large bandwidth of several GHz. We have used an input stage similar to the NINO circuit [9] that senses the differential current with a differential common gate cascode stage and provides the termination of the transmission line. The schematic of the receiver is presented in Figure 10.

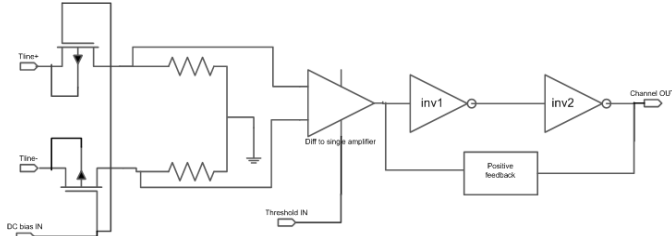


Figure 9 schematic of the line receiver with its dynamic asynchronous comparator output stage providing extremely fast digital signal edges

The receiver input stage biasing is provided directly by the static current of the transmission line of about 250 μ A. The output of the receiver input stage is sensed with a broadband differential to single ended amplifier stage whose output is converted into a fast digital CMOS level signal by a dynamic asynchronous positive feedback latch comparator stage which generates pulses edges of 50 ps to drive TDC inputs.

4) End of column logic:

The end of column circuitry comprises one receiver bank (9 receivers, one for each transmission line), one TDC bank (9 TDC's), address encoding circuits and the digital logic for processing the hit data ready for transmission off chip. For the prototype demonstrator the 32-bit DLL providing the 32 delayed clock signals for the hit registers in the TDC bank and one PLL providing a 320 MHz clock signal for the DLL are common to all end of line circuits. The TDC circuits used in the end of column logic is based on previous development done in 250 nm CMOS technology [10], and in 130 nm CMOS technology [11].

Each TDC consists of two 32-bit hit registers, one for the leading edge and one for the trailing edge of the hit, providing a double time stamping. The leading edge time stamp provides information of the hit arrival time and the trailing edge provides the additional input charge amplitude information needed to correct time walk.

The two 32-bit time stamps are encoded into 5-bit binary words. The double time stamp with coarse counter and address information are stored in a line buffer, which is then serialized and sent off chip.

Distributing DLL outputs to all the 40 columns is an issue as the load comprises 40 TDC banks and a long distance. This problem is solved by having in addition to a strong differential buffer at the output of the DLL a receiving buffer at the input of each TDC bank. The output of the DLL buffer is differential and is converted into single-ended only at the input buffer of each TDC bank. The hit registers use single-ended CMOS level signals. The hit register in the TDC are built of 32 D-type flip flops with rising edge trigger. The

output of the receiver cell provides a rising edge trigger for both leading and trailing edge hit registers.

The EOC circuits are outside the beam area and thus the radiation levels are very low. Therefore it looks like there is no need to use digital circuits protected against SEU effects or leaking currents in NMOS devices. Also, as the sensitive analogue circuits are in the pixels and use different power supply as the isolated EOC circuits, there is no need to use differential logic.

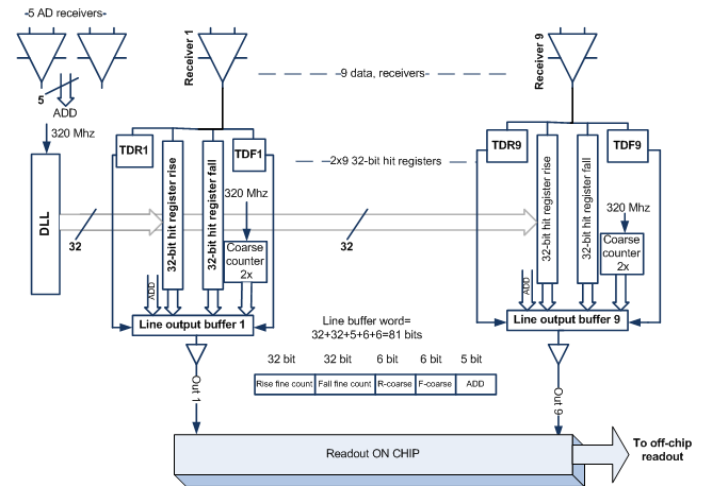


Figure 10 One end of column circuit as designed for the EOC demonstrator circuit

The clock frequency is 320 MHz resulting in a 3.125 ns period and a delay of a single delay cell of 97.66 ps.

EOC circuits have a very dense layout design since the receiver bank, the TDC bank and the digital circuits must fit inside a 300 μ m pixel wide periphery of each column.

The address bus has its own receiver bank (5 receivers, one for each address line) which provides the data required for the pixel address. All the data including the address and the time stamps are left non-coded in the demonstrator to give access to raw data.

In addition to the already mentioned circuits two trigger signals are generated from the hit signals to control the writing of data hit in the output line buffer.

VI. CONCLUSION

We have presented the challenges of ASIC development of the NA62 pixel Gigatracker and the current status of the circuit design of the pixel cells and bus system. Speed and noise specification are extremely challenging in terms of ASIC design. Two circuit demonstrators have been developed using complementary ASIC architectures which integrate TDC circuit in the pixel cell and in the end of column circuit. The demonstrator circuits will be submitted to fabrication end of 2008. Characterization of the demonstrators will help to select the best architecture and pixel cell. In particular timing performance and circuit robustness against digital noise are of the prime importance in the choice of the best approach.

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