Effect of carrier tunneling on the structure of Si nanowires fabricated by metal assisted etching

doi:10.1088/0957-4484/27/34/345301

Effect of carrier tunneling on the structure of Si nanowires fabricated by metal assisted etching

S J Rezvani[1,2], R Gunnella[1], D Neilson[1], L Boarino[2], L Croin[2], G Aprile[2], M Fretto[2], P Rizzi[3], D Antonioli[4] and N Pinto[1,5]

[1] Scuola di Scienze e Tecnologie, Sezione di Fisica, Università di Camerino, Camerino, Italy
[2] Istituto Nazionale di Ricerca Metrologica, INRiM, Torino, Italy
[3] Dipartimento di Chimica e Centro NIS, Università di Torino, Via Giuseppe Verdi, 8, Torin, Italy
[4] Dipartimento di Scienze e Innovazione Tecnologica (DISIT), Università del Piemonte Orientale, INSTM, UdR Alessandria, Viale Teresa Michel, 11, 15121, Alessandria, Italy
[5] INFN, Sezione di Perugia, Italy

Abstract

The metal assisted etching mechanism for Si nanowire fabrication, triggered by doping type and level and coupled with choice of metal catalyst, is still very poorly understood. We explain the different etching rates and porosities of wires we observe based on extensive experimental data, using a new empirical model we have developed. We establish as a key parameter, the tunneling through the space charge region (SCR) which is the result of the reduction of the SCR width by level of the Si wafer doping in the presence of the opposite biases of the p- and n-type wafers. This improved understanding should permit the fabrication of high quality wires with predesigned structural characteristics, which hitherto has not been possible.

Keywords: silicon, nanowire, metal assisted etching, fabrication, surface

1. Introduction

Silicon nanowires with typical diameters less than 100 nm have attracted attention during the last decade due to their exceptional optical and electrical properties, with important possible applications in optoelectronics, [1–4] biochemical sensing [5] and thermoelectronics [6]. For example optimal potential control in core shell crystalline Si wire structure makes Si nanowire an excellent candidate for the metal insulator semiconductor devices and tunnel field effect transistors [7, 8]. On the other hand the porous Si nanowires can be exploited in the sensing devices in which small volume allows effective control of the nanowire potential with a small input signal making it very sensitive while porous wire structure increases the surface area and hence the sensitivity of the device. Recently, it has been shown that in contrast to bulk porous silicon the porous silicon nanowires demonstrate a single electronic transport mechanism which depends on the pore size and internal structure [9]. This property combined with a tunable refractive index and band gap in the porous structure can lead to new generations of nanosolar cells with embedded quantum dots, high quality waveguides, nano-LEDs and field emitters.

While UHV deposition techniques like molecular beam epitaxy [10, 11] can have a precise controllability over the fabricating of Si nanowires, the technique of metal assisted chemical etching (MAcE) [12, 13] has significant advantages. These are its simplicity, possibility of large area nanowires fabrication and its low cost. In MAcE, the silicon wafer undergoes a reduction-oxidation process in a catalytic solu-tion (usually HF and H_2O_2) in the presence of metal particles or a metal layer [12–14].

Unfortunately fabrication of nanowires by MAcE is still imprecise and irreproducible [15]. For instance, using Ag nanoparticles as metal catalyst results in a large area of dissimilar wires, the structures of which are not predictable.

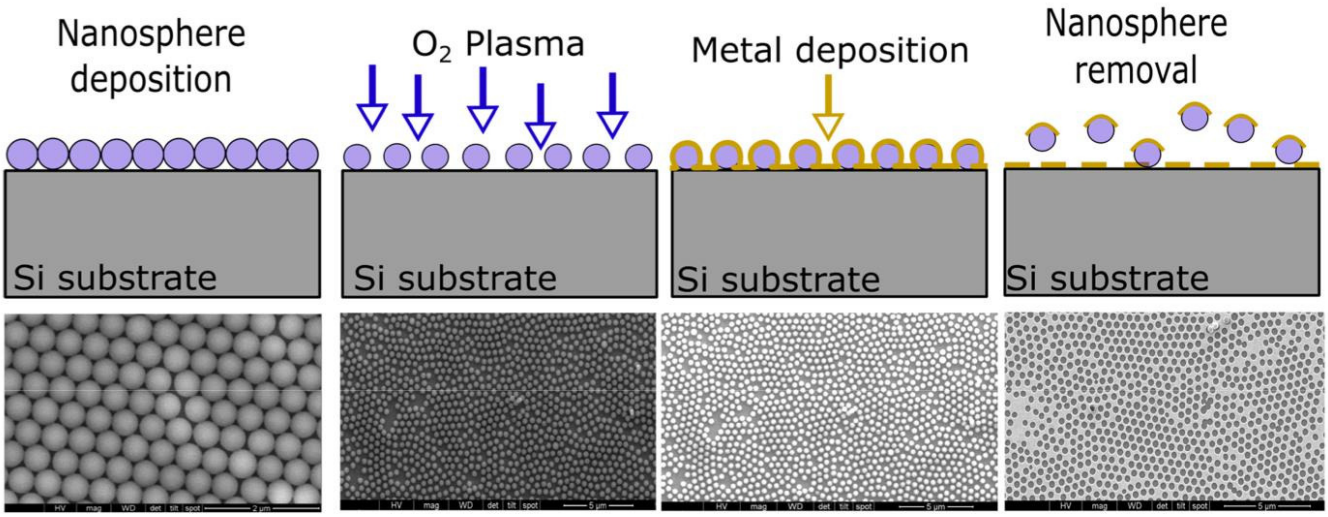

Figure 1. Schematics of the colloidal lithography (top) with the sequential SEM micro-graphs of resulting samples (bottom).

Existing theoretical models are only qualitative with respect to the effects of the doping of the Si wafer on the resulting wire structures. Experimental studies of the fabrication process lead to results that appear to be in mutual contradiction, as will be discussed later. These studies do partially explain the etching process mechanism, including the controllability of the porosity by oxidant concentration in catalytic solution. However the etching mechanism triggered by doping type and doping level, as well as the role of metal catalyst regarding the doping of the Si wafer, remains unexplained.

Here, we report on a complete and systematic experimental investigation of the different parameters affecting the etching process. This lead us to propose a mechanism that explains the variety of outcomes in the process as functions of (i) the substrate doping type, (ii) the substrate doping level and (iii) the metal catalyst.

2. Results and discussion

We fabricated nanowires, measured the etching depth using scanning electron microscopy (SEM) micrographs, analyzed the wire structures using high resolution transmission electron microscopy (HRTEM) and the composition by X-ray photo-electrons spectroscopy (XPS). We also measured for the first time the potential difference between the surfaces of the silicon wafer while under etching.

2.1. Fabrication

The fabrication process was metal assisted chemical etching using colloidal lithography (figure 1) with a lateral resolution of few nanometers. Silicon substrates of (100) orientation with four different p- (B doped) and n- (P doped) doping level with resistivities of 10-20 Ωcm and 0.01-0.02 Ωcm respec-tively, were first cleaned in acetone and deionized water, then dipped in 10% HF solution to remove native oxide. Then, polystyrene nanospheres, synthesized by emulsion poly-merization [16], with initial size of 140 nm, were deposited on the substrate and introduced into the plasma etching chamber for size reduction to a mean value of 90 nm, by a gas mixture of O_2 and Ar (figure 1). Afterwards, a 20 nm layer of Au was evaporated by an electron beam gun. Ag and Ni, deposited by thermal evaporation, were also used as catalysts for compar-ison with properties of Au. After that, the nanospheres were removed by sonication in deionized water, followed by dip-ping of the sample in a solution of $HF:H_2O_2:H_2O$ with the ratio of 3:1:1 using 50% HF and 30% H_2O_2 for 2, 4 and 6 minutes.

The MAcE process was performed at room temperature in the dark to avoid photo-generated holes. The samples were etched in a vessel containing a large volume of electrolyte (electrolyte/sample volume ratio ~10^4) to reduce the effect of HF/H_2O_2 exhaustion. The sample was stirred very slowly to make sure its contact with fresh solution. A total number of 9 samples of each doping type and doping level were fabricated (36 in total), 6 out of 9 of each set (a total of 24 out of 36), randomly chosen, underwent the analysis to ensure the reproducibility of the results.

2.2. Etching depth

Figure 2 shows a micrograph of different samples fabricated using different doping types and doping levels of Si wafers with a 20 nm Au catalyst etched for 6 minutes. In the table 1 the etching depths of the samples from the same wafer etched for 4 and 6 minutes are given and compared with the etching depth of samples fabricated with a 20 nm Ag catalyst layer, etched for 6 minutes.

The results in table 1 indicate a much higher etching depth for heavily p- and n-doped wafers, covered by Au. They indicate a slightly lower etching rate in n-type wafers compared with p-type. The ratios are unchanged for etching durations of 4 and 2 minutes. Our results are in disagreement with those reported by Li et al [17]. They reported that a comparison of lightly (1-10 Ωcm) and heavily (0.01-0.03 Ωcm) p-type doped Si wafer, covered with Au, shows only a small variation in etching rate of the fabricated wires.

However, our results for p-type wafers are in agreement with those of Cruze et al [18] who reported a much higher etching rate when Si wafer is heavily doped. The only agreement we observed with [17] is in the case of Ag catalyst. Both [17] and our results record a slight difference between heavily and lightly n- and p-type doped substrates. We found that with Ag catalyst the n-type wafers show a slightly smaller etching depth compared with the p-type. Additionally, the etching depth in general is much lower using Ag compared to the Au catalyst. These results show that the doping type and the doping level both significantly affect the etching process.

Comparison between our results from Au and Ag catalyst indicates that the process is also controlled by the metal catalyst. Previously it has been qualitatively suggested that the role of the metal catalyst would be injection of the holes, generated in the catalytic solution, into the valence band of the semiconductor [19]. This charge transport should depend strongly on the surface band bending of the Si caused by the surface states. References [19, 20] qualitatively discussed the electrochemical energy of the Si bands versus the redox potential of the system, and suggested that one side of the metal particles (Ag nanoparticles in their study) can act as a cathode and the other side as an anode, thereby creating a self generated field across the metal particles double layer [20]. They did not discuss, however, how this field generation

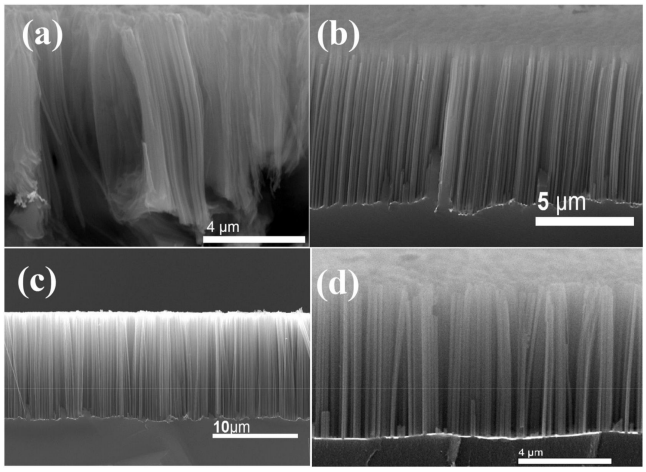

Figure 2. SEM images of Si wires prepared by etching Si(100) wafers having different doping levels evidencing the etching depth. (a) LD p-type; (b) LD n-type; (c) HD p-type; (d) HD n-type. Wires in figure (a) are similarly perpendicular to the substrate. This figure was chosen for better visibility of the self standing wires.The tilting is due to breakage of the sample for cross section preparation.

might affect the etching process modifying the energy band structure at the interface. On the other hand a recent model suggests that a net positive charge accumulated in the metal particle creates a potential, leading to initiation of the etching (see [21]). However, the proposed model do not explain the effect of metal type in the etching process.

To clarify the etching mechanism, we used a continuous metal film in place of nanoparticles to avoid diffusion of the particles in the solution. Use of a film permitted us to measure for the first time, an average voltage drop across Si wafer and the metal surfaces while dipped in the etching solution. The measurement was done using two Pt electrodes, one in the solution and the other contacted to the front surface of the wafer. In addition, an Al electrode was contacted to the back Si surface (figure 3). We measured an average $\Delta V \sim -500$ mV for Au and $\Delta V \sim -200$ mV for Ag film. The voltage drop was found to be independent of the doping type of the Si wafer. This measurement was repeated without a metal layer and no voltage drop was measured.

The measured voltage drop qualitatively confirms pre-vious suggestions (see [20, 21]) that the spontaneous reaction:

$$Si + 2\,H_2O_2 + 6\,HF \quad H_2SiF_6 + 4\,H_2O \qquad (1)$$

can convert the metal layer to act like a galvanic cell. The ΔV indicates that there is a net applied potential by metal to the substrate. The measured value, being in the range of the Au-Si/Ag-Si redox-valence potential difference, suggests that the generated bias can be related to this potential difference in presence of the electrolyte. Based on the model proposed by Peng et al [20], the applied potential can be generated by the negative induced charges on the metal surface due to proton gradient in the electrolyte solution. The surface accumulated negative charge induces a net positive charge in semicon-ductor which result in formation of the space charge region (SCR) at the metal-semiconductor interface. A net localized negative charge at the metal-semiconductor interface main-tains the p-type Si wafer in a forward like polarization and the n-type in a reverse like polarization. In both cases, a field is induced across the SCR at the interface of the semiconductor which results in a voltage drop at metal-semiconductor interface.

Thus, considering the discussion above, an etching mechanism analogous to the anodic electrochemical etching occurs. The difference among the etching rates depending on the substrate doping can be explained by considering the Schottky barrier created at the metal-semiconductor interface in the presence of the applied potential by the metal. In the standard theory of the metal-semiconductor junction, without

Table 1. Wires properties prepared using Au and Ag catalyst. From left to right: Si wafer doping (lightly doped (LD) and heavily doped (HD)); resistivity; dopant type; average wire length for different etching times. Lengths were determined from SEM vertical images.

Case	Wafer resistivity (Wcm)	dopant	Au 6 min (µm)	Au 4 min (µm)	Ag 6 min (µm)
LD p type	10-20	B	8.5	2.4	2.6
HD p type	0.01-0.02	B	11.5	5.14	2.51
LD n type	10-20	P	7.7	2.2	1.4
HD n type	0.01-0.02	P	9.5	4.3	1.5

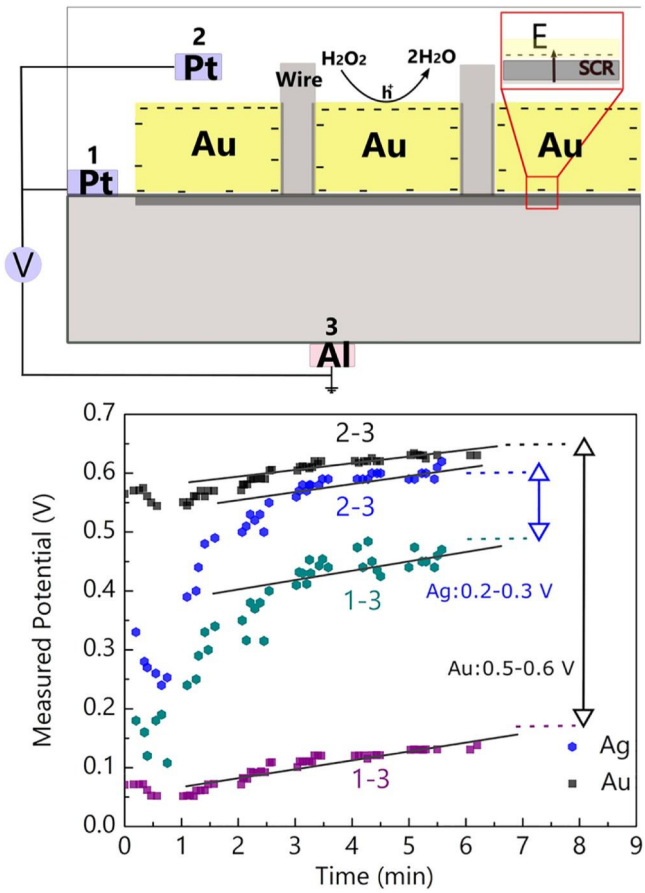

Figure 3. (Top) The potential measurement setup including two Pt electrodes, one in the catalytic solution and the other connected to the front surface of the Si wafer. An Al electrode is also connected to the back face of the Si wafer. (Bottom) The potential drop, ΔV, was measured between 2-3 and 1-3 electrodes using a double channel multimeter with 20 ms time delay between each measurement. In each run either electrode 1 or 2 was open. The voltage drop $\Delta V = -500$mV in case of Au and $\Delta V = -200$mV in case of Ag were measured. The potential drop directly measured from 1-2 electrodes was in microvolts range since both are in electrolytic solution and close together. The charge distribution in the metal layer is also shown along with the electric field across the SCR region created by the net charge at the anode side of the metal layer (inset).

the applied bias, the total current which is the summation of four distinct components is zero at equilibrium. These currents are shown in figure 4 (Top-left) in which I_1 and I_2 are the electron currents and I_3 and I_4 are hole currents flowing from the metal to semiconductor and vice versa, respectively. To explain the etching rate, the prominent current involved is that due to the holes flowing from the metal to semi-conductor (I_3).

For p-type Si, Au forms an almost ohmic junction (low barrier height ~0.2 eV) which facilitates hole currents from the metal to SC (I_3) resulting a high etching rate in presence of a forward bias. In highly doped p-Si, the hole current (I_3) can increase slightly by the reduction of the barrier height as suggested by Hochbaum [22] but the slight barrier height reduction cannot explain rates as high as observed by us. On the other hand, for n-type silicon wafers, the observed high etching rates cannot be explained by low density thermally generated holes at room temperature considering that all wafers were etched in dark and no photo-generated charge carriers were produced. Also, the barrier height mechanism cannot explain the n-type high etching rate, since if the barrier height controlled the rate as proposed by Hochbaum [22] and Geyer et al [23], then a reduction rather than an increase of the etching would be expected.

Our results suggest that in both p- and n-type Si wafers with the doping levels above 10^{18} cm^{-3}, as in our experiments, the barrier (SCR) width reduction, given by equation (2), is mostly responsible for controlling the etching rate [24, 25].

$$W = \sqrt{\frac{2\,_{r}\,_{0}(V_b - V)}{qN_A}} \qquad (2)$$

In this equation V is the net potential applied by the metal to the SCR, V_b is the built in potential, N_A is the acceptor concentration, $_r$ is the relative dielectric constant and $_0$ is the permittivity of free space. For the p-type wafer, increasing the doping level N_A up to 10^{18} cm^{-3} significantly reduces the SCR width and initiates tunneling of the charge carriers (electrons via F^-), in addition to the hole current increase (I_3) due to barrier height reduction. Such a tunneling mechanism results in a very high etching rate, as observed in our experiment.

For the n-type wafers, an explanation of the high etching rate is that the charge carriers are generated by direct tun-neling of the holes from the metal to the SC valence band due to the reduction of the barrier width and/or by electron tun-neling from the valence to the conduction band (electrical breakdown) due to the reverse bias. The breakdown is also favored by the SCR width reduction and leads to a high current density for the n-type wafers and hence high etching rate. However, in n-type Si, due to higher barrier and the holes being minority carriers the etching rate remains slightly less than in p-type Si. In both p- and n-type wafers, mass transport is the limiting mechanism of the charge carriers transport in the presence of an electrolyte. Etching occurs by reaching an equilibrium between charge and mass transport in the system [24].

With the metal films we employed, the induced field across SCR is quite uniform across the whole covered area due to the relatively uniform distribution of charge in the metal layer. We suggest that in the case of different geometries like nano particles, the highly localized fields in particle curvatures can significantly modify the etching process in specific directions.

Our results also indicates that the etching rate increases by time especially at the beginning. A similar trend is also seen in the measured potential. It may indicate a correlation between the measured potential and the etching rate such as SCR building up. However, the nature of the potential fluctuation especially in the first few minutes is not clear to us and requires further studies.

Turning to the type of metal catalyst as a controlling factor of the etching process, table 1 shows that using Au

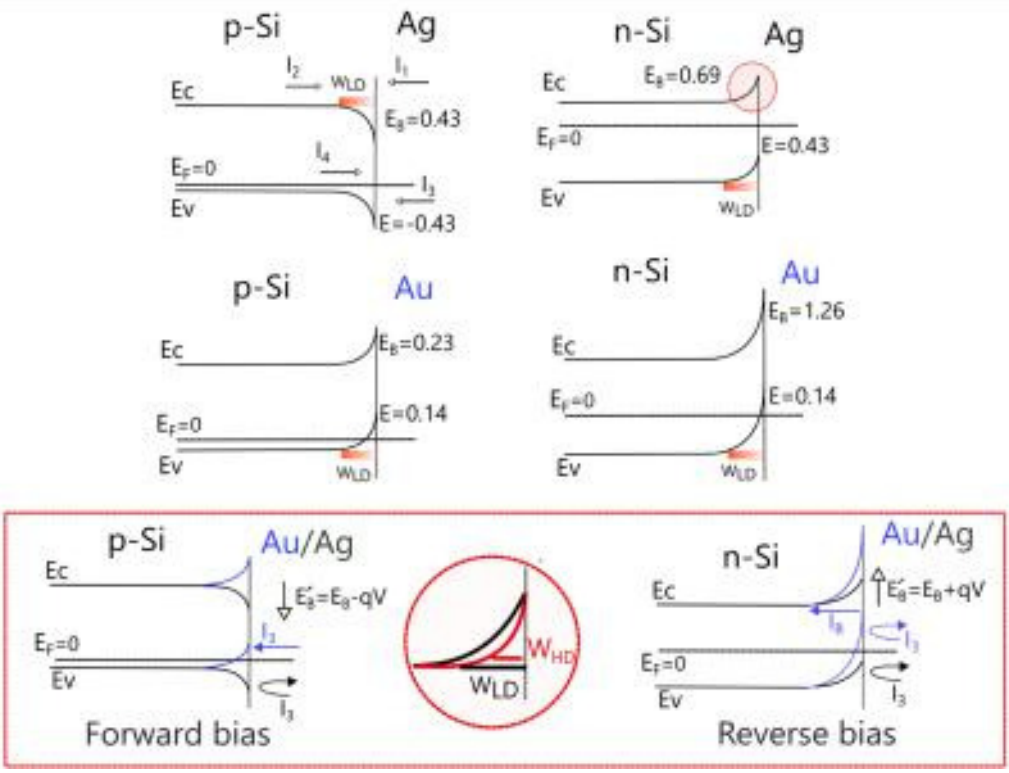

Figure 4. (Top) Schematic of Schottky barrier formation and the relevant band alignment for n- and p-type silicon junction with Au and Ag metals. The barrier height (E_B) and the energy of the valence band (E_v) is calculated using the values taken from [21]. Currents shown in the figure, I_1 and I_2, are electron currents from the metal to the semiconductor and vice versa, respectively; I_3 and I_4 are the analogous currents for holes. At equilibrium without an applied bias the summation of these currents is zero. (Bottom rectangle) The band alignments caused by the metal self generated potential (V) in presence of electrolyte. For n-type Si, in presence of a reverse bias, barrier heights (E'_B) in contact with both Au and Ag are increased as $E'_B = E_B+qV$ and the hole current from metal to SC (I_3) is hindered. For Au the breakdown I_B occurs, resulting in a high current density. For p-type Si, in presence of the forward bias, the barrier height decreases as $E'_B = E_B-qV$. Forward bias favors I_3 in case of Au while this current is minimized for Ag due to a contra alignment. In both p- and n-type Si, increasing the doping level reduces the barrier width (W shown in the red circle) and slightly decreases the E_B.

enhances the etching rate compared to Ag. There is also a minor dependence on the Si substrate doping level when using Ag. Low etching rate for p-type Si using Ag is expected due to its band alignment in forward bias (figure 4) which does not favor the hole current I_3 into the SC and hence, significantly reducing the etching rate. On the contrary, for the n-type with a reverse bias applied to the junction an etching rate similar to gold is expected. However, the very low etching rate observed for n-type along with the constant etching rate for different doping levels in both p- and n-type Si signifies the absence of the tunneling. From our measure-ment it was observed that Au applies a larger bias (higher drop) compared with the Ag. Looking at the redox potentials of the metal catalysts it is reasonable to assume that the current density (i.e the holes transport into the Si) depends on the redox potential (E°) of the metal catalyst,

$$Au^{+} + e^{-} Au \ (E^{\circ} = 1.5 \text{ ¸ } 1.68 \ SHE) \quad (3)$$

$$Ag^{+} + e^{-} Ag \ (E^{\circ} = 0.81 \ SHE) \quad (4)$$

Comparing the E° for Au and Ag, it can be deduced that more positive metal redox potential in the galvanic redox process [19] results in a higher bias applied to the SCR and hence, higher etching rates. Thus, the higher redox potential of Au compared with the Ag accounts for the higher etching rate observed experimentally. A high bias resulted from a high redox potential can also source the tunneling for heavily doped Si. With the lower bias induced by the low redox potential of Ag (as verified by our measurement), tunneling may not occur, which explains a similar etching rate between lightly doped and heavily doped Si substrates. We confirmed our hypothesis by using Ni which has a slightly negative redox potential E° = –0.26, having a similar work function to Au and hence similar barrier formation. We observed for Ni that as we had expected the etching rate was almost zero, regardless of the similar conventional band alignment to the Au. High neutralization of Ni^{+} in reaction with F^{-} ions could also reduce the etching rate.

2.3. Porous structure

High resolution scanning electron microscopy (HRSEM) micrographs show that all our nanowires are porous, in agreement with previous works [17, 22, 26]. In general, we found that the n-doped samples show a smoother surface compared to the p-doped samples. HRTEM analysis of the heavily p-doped samples reveals mesoporous nanowires with pore size of approximately 10 nm, containing silicon nano-crystals of 2-4 nm (figure 5). To check the depth of the

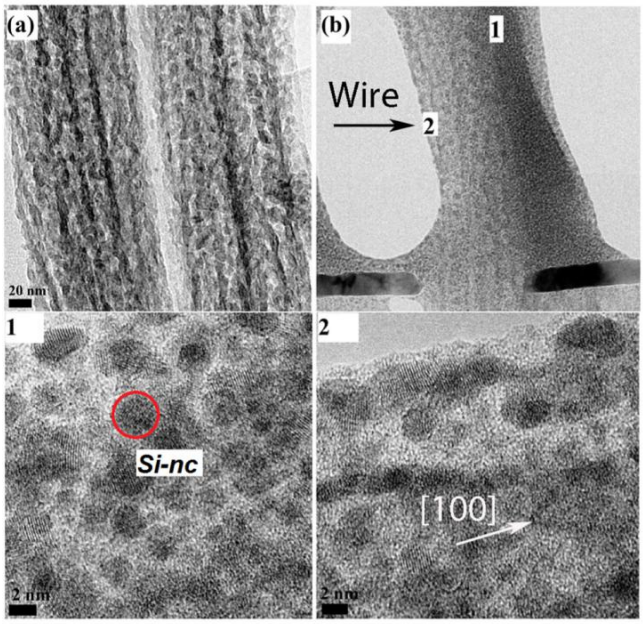

Figure 5. TEM image of the heavily p-type doped wire fabricated by using Au thin film catalyst. (a); (b): TEM evidencing the surface structure. Bottom photos are magnification of the region shown by numbers on panel b. Wire is mesoporous, containing silicon oxide with crystalline silicon dots embedded in it. The image from the surface (2) and close to core (1) shows similar structure with pore dimension of about 10 nm and Si NCs of 2-4 nm.

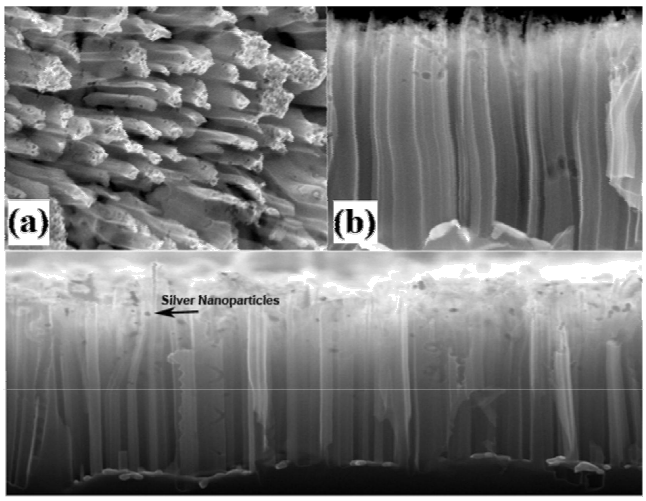

Figure 6. SEM images of the wires prepared using Ag catalyst; (a) n-doped and (b) p-doped. Larger pores are clearly visible on the wires surface. The huge pores on the wall are due to nucleation of the metal particle on the surface during the etching. A typical Ag particle remained on the wires wall is shown by the arrow.

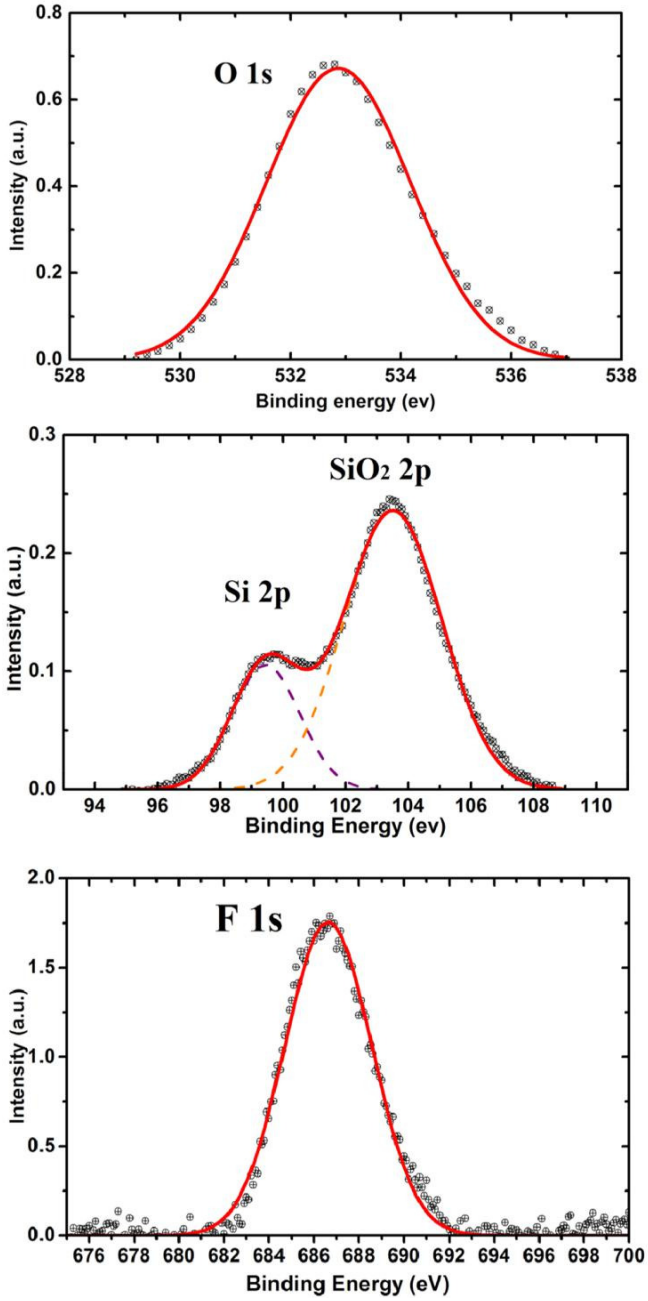

Figure 7. XPS spectra of the heavily p-doped Si nanowires using Au catalyst after 30 minutes of Ar sputtering, showing high concentra-tion of silicon oxide in deep layers of the wire with SiO_2:Si ratio of 3:1. This ratio is the same also for the surface layers. The presence of the fluorine in deep layers is the result of the passivated pore walls. The Fluorine peak was not observed in the surface layers.

porosity, a lamella was created in the longitudinal cross section of the wire. The cross section micrograph shows a wire completely porous up to the core. The structure of the wire near the core and near the surface are shown separately in figure 5.

Our proposed mechanism can explain the structure of the wires. Porosity of the sidewalls can occur via three distinct mechanisms:

First, the metal layer etches the sidewalls simultaneously during the etching process, thus forming the main pore structure of the samples. The pore size measured in the mesoporous structure of the heavily doped sample, confirms the presence of a narrow SCR and hence significant tunneling. Lehmann et al suggested in a related system that the meso-porosity structure was the result of the tunneling [24, 25]. In our proposal, larger pores (≅ 80 nm) on the wires formed using Ag would be the result of lack of tunneling.

Second, dispersed metal ions can nucleate on defect sites created by etching, becoming trapped in the pit and thus forming a metal particle. This process favors a deeper etching of the sidewalls [23] and larger pores. We have observed this effect for the Ag catalyst (figure 6).

Third, the self-standing Si wire in the solution continues to be etched with a much lower etching rate until the pore sidewalls become passivated by negative ions and the etching ceases [24]. To examine this effect, we carried out X-ray photoemission spectroscopy (XPS) on the heavily p-doped sample before and after 30 minutes of Ar sputtering. The XPS results from the surface layers (before sputtering) show that the wires consisted of silicon oxide and silicon with a 3:1 ratio (figure 7).

Our study of the deeper layers for these structures demonstrate for the first time the presence of fluorine (F^-), thus confirming the passivation of the pore sidewalls as proposed in [24] and by us. XPS of the deep layers also showed a similar ratio of oxygen and silicon, confirming that the porosity extends to deep layers.

3. Conclusion

In this work, we have discussed the metal assisted etching of doped Si substrate, considering the surface band bending at the metal-semiconductor interface in presence of a self generated bias applied to the Si wafer by the metal catalyst. Our results show that the self generated bias keeps the n-type wafer in reverse bias and the p-type wafer in forward bias. High etching rates for both p-type and n-type doping is a result of tunneling through the SCR region that is induced by this self generated bias. We demonstrate that both doping and metal catalyst control the wire structure and the pore size. Higher the doping level and catalyst redox potential, higher is the porosity with smaller pore size. On the contrary, etching of heavily doped Si in the presence of a low redox potential catalyst results in a micro-porous structure. The presence of F^- ions, observed only in deep layers, confirms that etching continues up to the point that the sidewalls are depleted by F^- ions. This established control over the structure should make possible the engineering of Si nanowires with predesigned structure.

Acknowledgments

This work is supported by the European Metrology Research Programme (EMRP), project SIB61 CRYSTAL. The EMRP is jointly funded by the EMRP participating countries within EURAMET and the European Union. This work is also partially funded by MIUR FIRB project THERMALSKIN grant RBFR10VZUG and by Camerino university project FAR 2012 CESEMN. Nanofacility (INRiM) is a laboratory supported by Compagnia di San Paolo Foundation.

References

[1] Canham L T 1990 Appl. Phys. Lett. 57 1046–8
[2] Kang Z, Tsang C, Wong N-B, Zhang Z and Lee S-T 2007 J. Am. Chem. Soc. 129 12090–1
[3] Pavesi L, Dal Negro L, Mazzoleni C, Franzo G and Priolo F 2000 Nature 408 440–4
[4] Fang H, Li X, Song S, Xu Y and Zhu J 2008 Fabrication of slantingly-aligned silicon nanowire arrays for solar cell applications Nanotechnology 25 255703
[5] Lin V, Motesharei K, Dancil K, Sailor M and Ghadiri M 1997 Science (New York) 278 840–3
[6] Hochbaum A, Chen R, Delgado R, Liang W, Garnett E, Najarian M, Majumdar A and Yang P 2008 Nature 451 163–7
[7] Björk M T, Knoch J, Schmid H, Riel H and Riess W 2008 Silicon nanowire tunneling field-effect transistors Appl. Phys. Lett. 92 193504
[8] Singh N, Buddharaju K D, Agarwal A, Rustagi S C, Lo G Q, Balasubramanian N and Kwong D L 2008 Fully gate-all-around silicon nanowire CMOS devices Solid State Technol. 51 34–7
[9] Rezvani S J, Pinto N, Enrico E, D'Ortenzi L, Chiodoni A and Boarino L 2016 Thermally activated tunneling in porous silicon nanowires with embedded si quantum dots J. Phys. D: Appl. Phys. 49 105104
[10] Shakthivel D and Raghavan S 2012 J. Appl. Phys. 112 1–5
[11] Wen C-Y, Reuter M, Tersoff J, Stach E and Ross F 2010 Nano Lett. 10 514–9
[12] Huang Z, Geyer N, Werner P, De Boor J and Gösele U 2011 Metal-assisted chemical etching of silicon: a review Adv. Mater. 23 285–308
[13] Chartier C, Bastide S and Lévy-Clément C 2008 Metal-assisted chemical etching of silicon in $HF–H_2O_2$ Electrochim. Acta 53 5509–16
[14] Shin J C et al 2012 Porosity control in metal-assisted chemical etching of degenerately doped silicon nanowires Nanotechnology 23 305304
[15] Huang Z P, Geyer N, Liu L F, Li M Y and Zhong P 2010 Metal-assisted electrochemical etching of silicon Nanotechnology 21 465301
[16] Antonioli D, Deregibus S, Panzarasa G, Sparnacci K, Laus M, Berti L, Frezza L, Gambini M, Boarino L and Enrico E 2012 PTFEPMMA coreshell colloidal particles as building blocks for self assembled opals: synthesis, properties and optical response Polym. Int. 61 1294–301
[17] Li X and Bohn P W 2000 Appl. Phys. Lett. 77 2572
[18] Cruz S, Honig-d'Orville A and Muller J 2005 J. Electrochem. Soc. 152 C148–24
[19] Peng K-Q, Hu J-J, Yan Y-J, Wu Y, Fang H, Xu Y, Lee S-T and Zhu J 2006 Adv. Funct. Mater. 16 387–94
[20] Peng K, Lu A, Zhang R and Lee S-T 2008 Adv. Funct. Mater. 18 3026–35
[21] Kolasinski K W 2014 The mechanism of galvanic/metal-assisted etching of silicon Nanoscale Res. Lett. 9 432
[22] Hochbaum A, Gargas D, Hwang Y and Yang P 2009 Nano Lett. 9 3550–4
[23] Geyer N, Fuhrmann B, Leipner H and Werner P 2013 ACS App. Mater. Interfaces 5 4302–8
[24] Lehmann V 1993 J. Electrochem. Soc. 140 2836–43
[25] Lehmann V 1999 J. Electrochem. Soc. 146 2968–75
[26] Huang Z, Zhang X, Reiche M, Liu L, Lee W, Shimizu T, Senz S and Gosele U 2008 Extended arrays of vertically aligned sub-10 nm diameter [100] si nanowires by metal-assisted chemical etching Nano Lett. 8 3046–51