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Design and characterization of a 64 channels ASIC front-end electronics for high-flux particle beam detectors

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ABSTRACT

A new wide-input range 64-channels current-to-frequency converter ASIC has been developed and characterized for applications in beam monitoring of therapeutic particle beams. This chip, named TERA09, has been designed to extend the input current range, compared to the previous versions of the chip, for dealing with high-flux pulsed beams. A particular care was devoted in achieving a good conversion linearity over a wide bipolar input current range. Using a charge quantum of 200 fC, a linearity within ±2% for an input current range between 3 nA and 12 μA is obtained for individual channels, with a gain spread among the channels of about 3%. By connecting all the 64 channels of the chip to a common input, the current range can be increased 64 times preserving a linearity within ±3% in the range between and 20 μA and 750 μA.

Keywords: Readout electronics; Current-to-frequency converter; Radiotherapy; Hadrontherapy; Charged particles; Ionization chambers.

1. INTRODUCTION

In radiation therapy, several techniques have been proposed in recent years to achieve a highly conformal delivery of the dose to the tumor target while sparing the healthy tissues. Such techniques require beam monitoring systems providing a fast and precise qualification of the therapeutic beam during the irradiation. These systems are typically composed by sets of parallel plate ionization chambers with different segmentations of the electrodes to provide spatial information.

Since many years, our group has been committed to the development of a family of multi-purpose, multi-channel ASIC chips, called TERA, to read out the charge produced in ionization detectors [1-3]. Tailored for clinical applications, the TERA chips were used in several clinical devices both for quality control in radiotherapy [4] and for beam monitoring in particle therapy facilities [5-7]. They are all based on the recycling integrator principle [8] to convert the input charge into pulse counts, or equivalently the input current into a pulse count frequency, each count corresponding to a fixed quantum of charge. This conversion method offers several advantages as the intrinsic lack of deadtime and the very good linearity up to the maximum conversion frequency. Also, the charge collected at any input channel can be sampled asynchronously with the conversion operations by simply reading the corresponding counter.

The previous version of the chip, TERA08, features 64 channels operating in parallel, each accepting input currents of both polarities and implementing a 32 bits counter with up/down counting capability [3]. TERA08 operates with a clock frequency of 100 MHz and a maximum conversion frequency of 20 MHz. Thus, using a charge quantum of 200 fC, the maximum current that a channel can convert without saturation is about 4 μA. This quantity is well above the typical currents of hundreds of nA measured in the present facilities for particle therapy. However, this limit will be too severe for the pulsed beam structure provided by the next generation of accelerators where, with the aim of reducing the complexity and increasing the performance of the machines, new accelerating technologies are exploited [9-12]. Short beam pulses of 1-10 μs duration with a repetition rate of 1 kHz or less will replace the almost constant beam flux used in the present clinical facilities, leading to an effective beam duty cycle two to three orders of magnitude smaller. Thus, to achieve a similar dose rate, the beam flux in each pulse will increase accordingly.

A simple method to increase the current range of the TERA08 was tested recently. It consisted of splitting evenly the input current of a detector element into several readout channels and adding up the counts of these channels to reconstruct the input current. It was shown [13] that this method allows to increase the maximum input current up to 64 times, when all 64

channels are used, preserving the good linearity achieved with the individual channels and with a limited increase in the standard deviation of the measurement. Nevertheless, there are drawbacks with this method; one is the lower number of detector elements which can be read out with a chip, the second is the necessity of reading out the values of a large number of counters, up to 64, and perform their sum. Both affect the versatility of the chip and strongly limit the range of application of TERA08. In addition, a 64 increase in the dynamic range could not be sufficient for the target application.
This paper presents the last version of the chip, named TERA09, designed to overcome these limitations. The charge-to-frequency converter has been improved in order to obtain a larger maximum conversion frequency. Moreover, the chip automatically calculates the partial and total sum of the counter values, which can be directly accessed in dedicated registers. In the design process, special care has been devoted in maintaining as much as possible the backward compatibility such that the new chip can replace the older versions in any of the current devices with small impact on the acquisition system and on the power supply. The results of the tests, presented in the last part of the paper, indicate the possibility to achieve an increase of about two orders of magnitude in dynamic range compared to the TERA08 without a significant loss in sensitivity and linearity, thus adding to this version the additional flexibility to extend its use to high-flux particle beams applications.

2. THE TERA09 CIRCUIT ARCHITECTURE

Fig.1 shows the architecture of the chip. It contains 64 identical channels equipped with a current-to-pulse-frequency converter, described in detail later, followed by a 32-bit counter. Currents of both polarities can be converted, leading to increments or decrements of the counters depending on the current polarity.
The readout of the counters can be done independently from the operations of the converters. By asserting a common external *latch* signal the content of all the counters are loaded simultaneously in 32-bit registers. This operation does not stop the activity of the counter, thus there is no dead time due to the readout.
An integrated system of adders triggered by the *latch* signal provides the sum of groups of 4, 16 and 64 channels. These values are stored in additional 34-, 36-, and 38-bit wide registers. Any of these registers can be addressed via seven digital *Channel Select* lines and read out on a 38-bit output bus through a multiplexer. This system allows to read directly the sum of the counters of 4,16 or 64 channels if, in order to increase the dynamic range, the input current is split among the channels, as explained in the previous section.

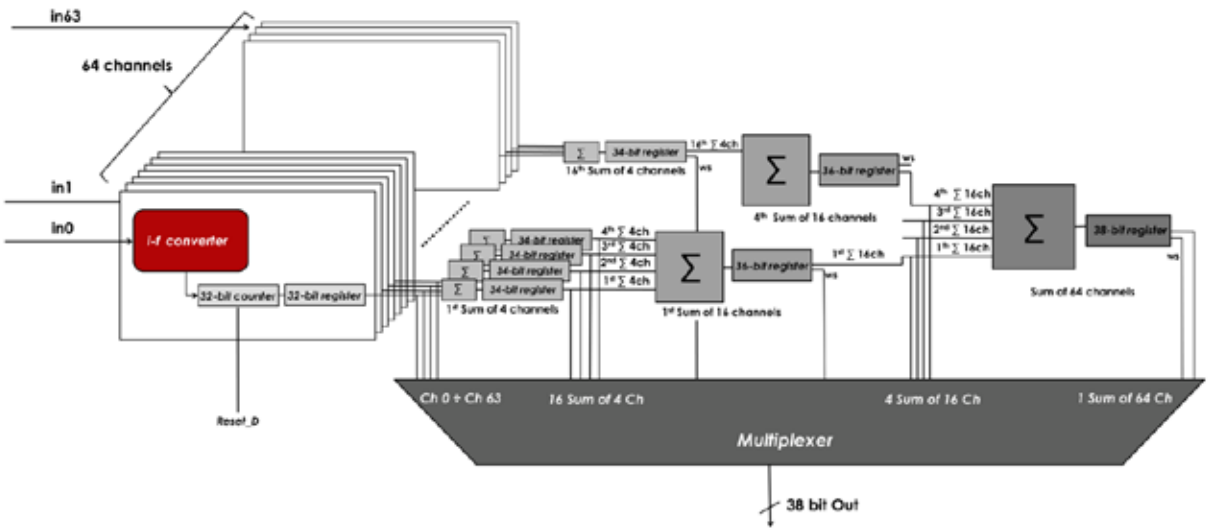

Fig. 1: Schematic layout of the TERA09 chip

Particular care has been taken in preventing the overflows of the registers to corrupt the corresponding sums. Indeed, the converter was designed to operate at the maximum conversion frequency of 80 MHz; in this limit condition, the counter 32-bit capacity will be exceeded, and the counter will reset to the starting value, approximately every 50 seconds. Such a condition is easily identified and corrected for if each individual channel is acquired separately, but may be more difficult to identify and correct when only the sum of a large number of channels is acquired. To identify in advance possible flips of individual counters, an output warning signal *ws* was implemented which is set whenever any of the 64 counters exceeds half of its capacity (see Fig. 1). When such condition occurs, the asynchronous digital *reset_D* can be used to zero all the counters soon after the *latch* signal.

The converter of TERA09 is based on the charge recycling technique and is implemented as shown in Fig.2.

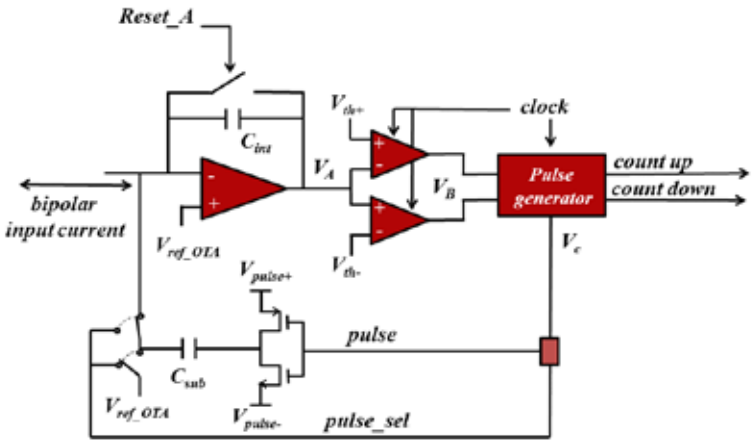

Fig 2: Layout of the TERA09 electrical current to pulse converter.

The input current is integrated over a 1.2 pF capacitor C_{int} via a folded-cascode operational transconductance amplifier (OTA). The output voltage V_A increases when the current exits from the chip (negative current) and vice versa. This voltage is compared with two fixed thresholds, V_{th+} and V_{th-}, by two synchronous comparators. Whenever the comparator input voltage crosses the threshold, the corresponding comparator sets a logic level 1 at one of the input V_B of the pulse generator (PG). When one of its inputs goes high, the PG generates a pulse V_C with a duration of 2 clock cycles that sends a current pulse with polarity opposite to the input current to discharge of the capacitor C_{int}. The pulse adds or subtracts a fixed amount of charge Qc, depending on the outputs of the comparators; this results in a change of voltage across V_A given by Q_C/C_{int}. In parallel, the PG sends an increment or a decrement signal to the counter. The waveforms of these signals are shown in Fig. 3 for the case of a steady negative current.

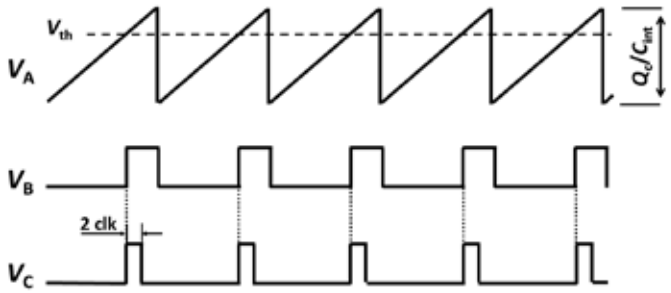

Fig 3: Voltage waveforms at the output of the charge integrator (V_A), the comparator (V_B) and the pulse generator (V_C) for a constant negative input current.

The circuit for the discharge of the integrating capacitor is shown in Fig.4.

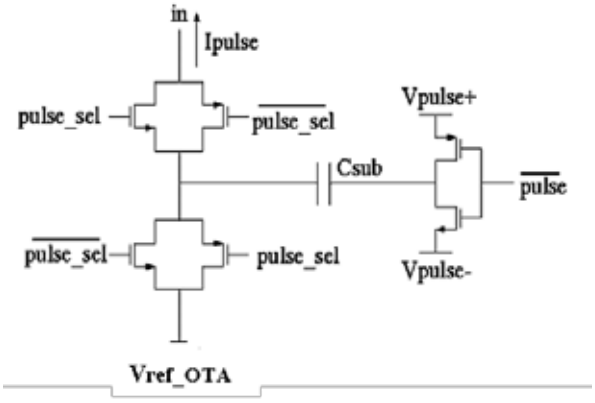

Fig 4: Circuit for the discharge of the integrating capacitor.

The pulse V_c is split in two pulse signals, *pulse* and *pulse_sel*, which are delayed one relative to the other. The first signal is used to send a voltage pulse to a 200 fF capacitor C_{sub}, whose amplitude is given by the difference $\Delta V = (V_{pulse+} -$

V_{pulse-}) which can be selected in the range between 0.25 and 3.3 V. At the edges of the pulse, the capacitor generates two δ-like current pulses of equal absolute value and opposite polarity, each with an integrated absolute charge given by

$$Q_c = C_{sub} \cdot \Delta V \quad (1)$$

Depending on the value set for ΔV, the charge quantum can therefore be selected in the range between 50 fC and 660 fC. One of the two current pulses is used to add either a positive or a negative charge quantum to C_{int} while the other is discharged toward the reference voltage of the OTA (V_{ref_OTA}). The selection is achieved by acting on the two CMOS switches via the *pulse_sel* signal. As an example, the waveforms shown in Fig. 5 lead to a positive charge quantum being added to C_{int}.

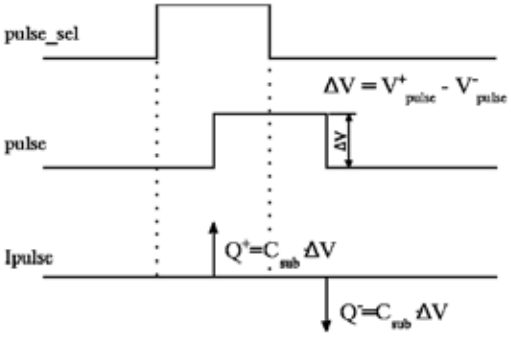

Fig 5: Example of voltage waveforms of the two pulses used by the circuit for the discharge of the integrating capacitor.

It should be noted that the voltage across the switches is always equal to the OTA reference, thus limiting the leak of charge through the switch. Another factor which could limit the resolution of the circuit is the charge injected by the parasitic capacitors of the switches. This charge is minimized by the use of CMOS switches and by choosing the minimum size for the transistors. Finally, the integration capacitors of all channels can also be fully discharged via the *Reset_A* common digital input.

The total charge collected at the input of the channel in a given time interval is given by the number of pulses generated by the PG in the same time interval, measured as the increment or the decrement of the counter, multiplied by the value of the charge quantum *Qc*. For an average input current I_{in}, the average output frequency *f* of the converter is given by

$$f = \frac{I_{in}}{Q_C} \quad (2)$$

All the operations described above are synchronized to an external master clock and supervised via a Moore-style finite state machine. Since four clock cycles are required to perform the C_{int} discharge sequence, the maximum conversion frequency is 1/4 of the master clock frequency. The chip has been designed to operate at a maximum clock frequency of 320 MHz; in this condition, the maximum output frequency of the converter is thus 80 MHz, an increase of a factor four compared to the predecessor.

Forty chips TERA09 were produced in the CMOS 0.35 µm technology by AMS taking advantage of a Multi Project Wafer organized by Europractice [14]. The chips, whose size is 4.68 x 5.8 mm^2, were encapsulated in an MQFP 160 package prior to delivery. In the following, the results of the tests performed on the chips are reported.

3. Experimental setup

The experimental setup used to characterize the ASICs was based on a National Instrument PXI chassis with a 7813R FPGA board, interfaced to the host PC using the LabVIEW FPGA software toolkit [15].
A custom test board was prepared containing a socket for housing the chip, the circuits for adapting the CMOS digital levels to the TTL levels of the DAQ board and all the voltages needed to operate the chip. The clock signal could be either generated on board through an LVDS voltage controlled oscillator or fed from an external unit. Finally, a connector allowed to inject a current separately in each input channel of the chip.
For some of the tests, a voltage generator was used to inject a precise steady current, either into a single channel or distributing it evenly in parallel to all the 64 channels. In the first case the source was connected to the input via a 10 MΩ resistor. The configuration for the parallel connection is represented in Fig. 6. It was previously shown [13] that the connection of groups of channels to a common input is only possible through 10 MΩ resistors, high enough to limit to a negligible value the offset currents which originate from the small voltage offsets of the input stages of the channels. In this case the input impedance seen by the generator amounts to 10/64 MΩ. A simple fan-in board with SMD resistors was prepared for this purpose.

The Keithley 2400 voltage generator was used, which provides a precise voltage source in the range between 1 mV and 211 V and is current limited at high voltages. For higher currents, we used a Bertan 323 model HV power supply, providing a voltage source up to 3 kV.

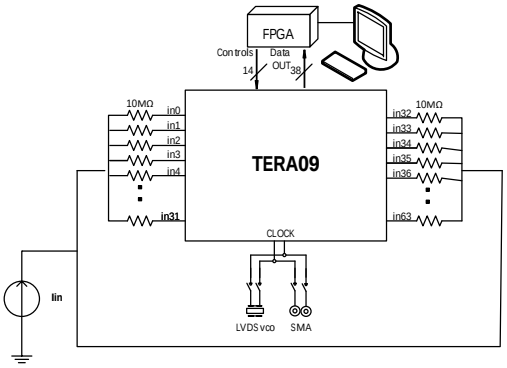

Fig 6: Schematic representation of the acquisition setup where 64 channels are connected in parallel to the current source.

4. TEST RESULTS

TERA09 was designed to achieve a good linearity over a large input current range, therefore the tests were mainly addressed to verify this feature. At first, this section describes the performance of the individual channels in terms of gain uniformity, background current and range of linearity. Afterwards, the linearity over the extended input range is presented with the inputs rearranged as shown in Fig. 6.

The basic functionality of the chips was checked by injecting a steady current in individual channels selected randomly and by measuring the corresponding number of counts. This check was repeated several times increasing the clock frequency. It was not possible to reach the maximum value of 320 MHz because the behavior of the chips was becoming very unstable at frequencies above 280 MHz. The problem was investigated in detail and was found to be related to the cross-talk between digital signals of the chips and the clock signal on the test board. The results reported in this paper were obtained with a 250 MHz clock, corresponding to a maximum counter increment frequency of 62.5 MHz, and should be considered as conservative in terms of the measured dynamic range. All the chips were found to be working and providing similar number of counts. One of them was selected randomly for the additional tests reported in the following.

As a preliminary step, for each value of the charge quantum Q_C used in the tests, a calibration procedure was adopted. The external reference voltages V_{pulse+} and V_{pulse-}, common to all the channels, were set acting on trimmers provided on the test board, according to the prescriptions of equation (1). The charge quantum of each channel was then derived, applying equation (2), by injecting channel by channel a steady current of 1 μA and measuring the corresponding counter frequency. The value, averaged over all the channels, was found to deviate by a few percent from the expected value, well within the tolerance of the capacitance values of C_{sub} which, for the used technology, is specified to be ±10%. The small deviation of the chip average charge quantum was corrected by adjusting the external reference voltages.

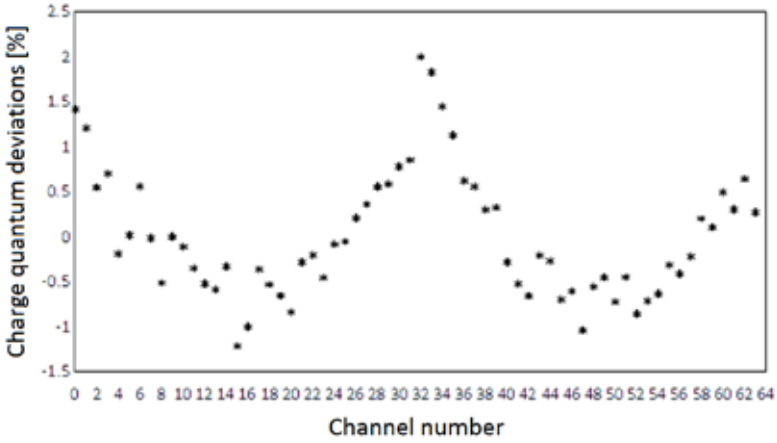

Fig. 7: Charge quantum relative deviations as a function of the input channel, obtained from 1μA input current measurements. Channels are numbered from 0 to 63.

Figure 7 shows the deviation of the charge quantum from the average as a function of the input channel number for a Q_C average value of 200 fC. This figure indicates that the gain uniformity across the channels of the chip is around 3%. A symmetric structure can be noticed where the trend observed in channels 0 to 31 appears to be similar to that observed in channels 32 to 63. This similarity may originate from the geometric arrangement of the channels in the chip, where the two groups of channels are positioned symmetrically along two opposite edges. Similar results are obtained at different values of Q_C, as expected considering that the relative deviation of the charge quantum is mainly proportional to the relative deviation of the capacitance of C_{sub}.

The background current was measured by acquiring data with the inputs of the chip unconnected. The measurement was repeated for charge quantum values ranging from 50 fC to 600 fC in 50 fC steps. The results, shown in Fig. 8, are expressed in terms of counts per second, where the following rule was adopted: the number of counts is assigned a positive sign when the counter is incrementing (i.e. for negative input currents) and a negative sign when the counter is decrementing (i.e. for positive input currents).

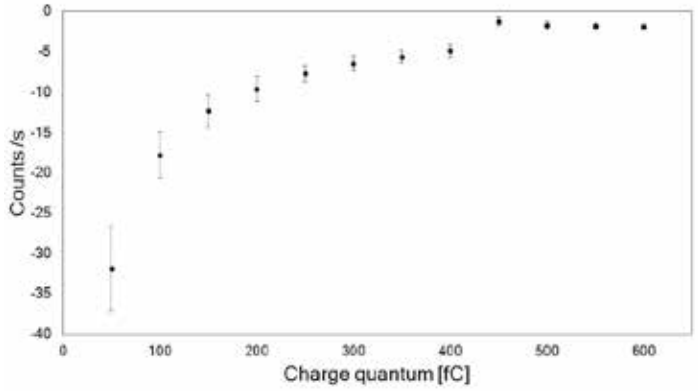

Fig. 8: Average background frequency as a function of the charge quantum Q_c. The vertical bar indicates the standard deviation of the 64 channels of the chip.

As expected, the result scales approximately with the charge quantum value. For a value of 200 fC, a typical choice for beam monitoring in particle therapy [16], an average background of about -10 counts per second is observed, corresponding to a positive pedestal current of 2 pA, almost two orders of magnitude smaller than the minimum currents measured in clinical applications. For the analysis presented in the following, the charge quantum was fixed to 200 fC, and the corresponding values of the pedestal of each input channel were stored and subtracted from the data in all the measurements.

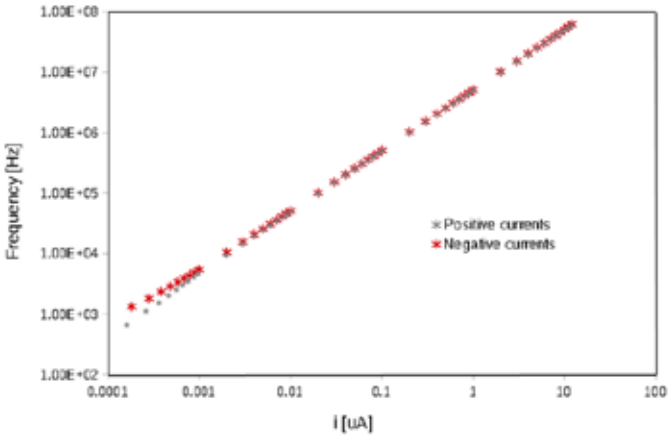

Fig. 9: Absolute value of the count frequency as a function of the absolute value of the input current for a single channel for a 200 fC charge quantum. Positive and negative currents are shown separately.

Fig.9 shows the absolute value of the counter frequency as a function of the absolute value of the input current for a typical channel of the chip, where positive and negative currents are shown separately. The measurement was performed for an input current ranging between ±80 pA and ±12 µA and the results were fitted to a line separately for positive and negative currents. The relative deviations from linearity as a function of the input current are reported in Fig. 10 with a vertical scale limited to ±2.5%. A good linearity is observed with deviations well within ±1% for most of the range except

for low absolute values of the input current, where it is found that the deviation exceeds 2% below 3 nA. For comparison, a maximum deviation from linearity of 1.5% was reported in the range 500 pA to 3 μA for the chip TERA08 [3].
As anticipated, TERA09 extends considerably the input current range compared to its predecessor. The worse linearity, compared to TERA08, at very small input currents was unexpected and may originate from leakage currents in the test board used for the measurements. The compact front-end printed circuit board for TERA09, currently under development, will be designed to overcome this problem.

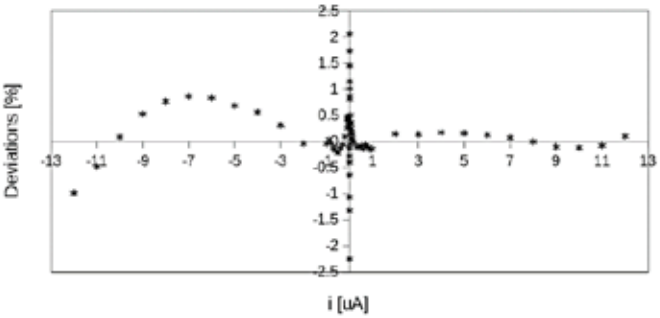

Fig. 10: Relative deviation from linearity as a function of the input current for the measurements reported in Fig. 9.

As explained in the previous sections, by reducing the number detector elements that can be served by a chip, the dynamic range can be further extended by splitting evenly the current through several channels of the chip and by reading out the sum of the corresponding counters. For example, reducing to 16 detector elements, the dynamic range is fourfold increased. All the results which follow were aimed at probing the performance with such arrangement and were obtained connecting all the 64 channels of the chip to the same current source, as shown in Fig. 6.

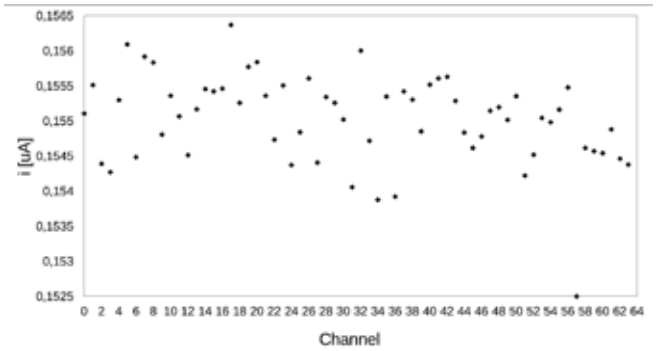

Fig. 11: Distribution of a 10 μA input current among the 64 channels of the chip. Channels are numbered from 0 to 63.

Figure 11 shows the current measured by each channel when a current of 10 μA was injected in the system. To convert the frequency of counts of each channel into current, equation (2) was used applying the channel-by-channel variations of gain of Fig. 7. The results indicate that the current is uniform across the channels with a maximum deviation of ±1%, compatible with the tolerance of the 10 MΩ resistors connected to each input.
The linearity obtained with this arrangement was tested, using a charge quantum of 200 fC, in a range of currents between ±10 μA and ±750 μA, yielding to the results reported in Fig. 12. The corresponding deviation from linearity, obtained with the same method as for the single input channel, is shown in Fig. 13 with a vertical scale limited to ±4%.

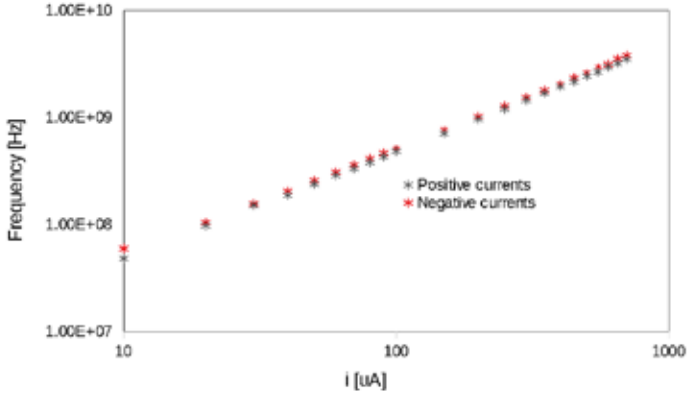

Fig. 12: Absolute value of the count frequency as a function of the absolute value of the input current for the sum of 64 channels, as described in the text. Positive and negative currents are shown separately.

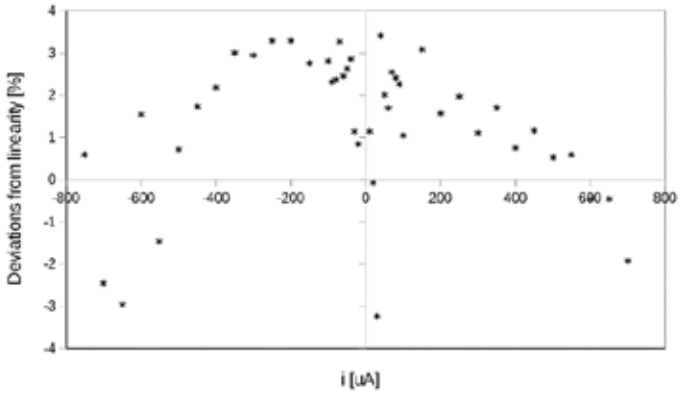

Fig. 13: Relative deviation from linearity as a function of the input current for the sum of 64 channels reported in Fig. 12.

It is found that a linearity better than ±3% can be achieved in a range of currents between 20 μA and 750 μA for both current polarities.

CONCLUSIONS

A new design of the 64 channels TERA front-end readout ASIC, named TERA09, has been presented. Each channel features a current-to-frequency converter followed by a 32-bit counter. Compared to the previous versions, the chip was designed to extend the current range for applications of beam monitoring of clinical pulsed particle beams. This was achieved by improving the maximum frequency of the current-to-frequency converter and by providing the possibility to access the sum of the counters of groups of channels directly on chip.

Using a charge sensitivity of 200 fC, the gain uniformity across the channels of the chip was found to be within 3%, with a background current of approximately 2 pA. It was shown that the chip can be adapted to read out currents from few nA to several hundreds of μA, with deviations from linearity at the percent level. This input range corresponds to a dynamic range of almost 6 orders of magnitude, an increase of two orders of magnitude compared to its predecessors.

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