Design of a 64 channels current-to-frequency converter ASIC, front-end electronics for high intensity particle beam detectors

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***Abstract*—A new wide-input dynamic range, 64-channels current-to-frequency converter ASIC has been designed and is now under characterization. This chip, nicknamed TERA09, has been realized to equip the front-end readout electronics for the new generation of beam monitor chambers for particle therapy applications. In this field, the trend in the accelerator development is moving toward compact solutions providing high-intensity pulsed-beams. However, such a high intensity will saturate the present readout of the beam monitor chambers. In order to deal with the technology innovations in the particle therapy, the chip described in this work is able to cope with a higher maximum intensity while keeping high resolution by working on a six orders of magnitude conversion-linearity zone (hundreds of pA to hundreds of μA), with a gain spread in the order of 1-3% (r.m.s.), with a 200fC charge resolution.**

Keywords—Readout electronics; Current-to-frequency converter; Radiotherapy; Hadrontherapy; Charged particles; Ionization chambers.

I. INTRODUCTION

The new generations of accelerators for particle therapy are moving towards compact accelerators systems that allow fast energy change of the beam particles, exploiting new technologies like laser-driven acceleration [1,2] and cyclinacs [3]. From the beam monitoring point of view, the change in the temporal beam structure, that, for these machines, moves from a semi-constant to a pulsed short bunch of particles (1-10 μs pulses with an average current per pulse, expected in the ionization chambers, of 1-25 μA), with repetition rates in the order of kHz, imposes new challenges. These short beam pulses have a high intensity, which need to be measured precisely in order to determine the dose released to the patient during the treatment.

The ionization chambers remain one of the most common choice as beam monitor detectors in particle therapy [4,5] and the reason is related to their simple and robust structure that minimally interacts with the beam. This simplicity has to deal with the high intensity pulsed beams which could imply efficiency reduction due to instantaneous ions recombination into the gaseous sensible volume [6]. The front-end electronics associated to the detectors is another point to be improved. With this target, the Experimental Physics Department (University of Turin) of and the Turin section of the National Institute of Nuclear Physics continued its decennial work on the design of multi-purpose readout chips for ionization monitor chamber applied in medical treatment facilities [4,7,8].

In this paper, we present the last version of the Application Specific Integrated Circuit (ASIC), which has been designed by our group, in collaboration with the DE.TEC.TOR. S.r.l. Devices and Technologies (a University of Turin spin-off company). This chip, named TERA09, currently under characterization, features a dynamic range increase of three orders of magnitude, compared to to its predecessor [9], without loss in sensitivity. This adds to this ASIC the flexibility to extend its use to high-intensity particle beams applications.

II. CIRCUIT ARCHITECTURE

The TERA09 ASIC is a current to frequency converter with 64 input channels that has the intrinsic capability of adapting the readout to an extended range of input currents, from hundreds of pA to hundreds of μA (i.e. a 6 orders of magnitude dynamic range), and with channel-to-channel gain deviations at the percent level. The whole architecture of the TERA09 chip can be subdivided in two parts, the input channels and the pulse count and sum logic.

A. The TERA09 channel

The TERA09 channel architecture is based on the charge recycling technique. As shown in Fig.1, the input current is integrated over a capacitor Cint via an operational transconductance amplifier (OTA), in a Folded Cascode architecture. The output voltage is compared with two fixed thresholds by two synchronous comparators. Whenever the comparator input voltage crosses the threshold, the corresponding comparator sets a level at the input of the pulse generator (PG). As soon as an input level is set, PG sends to the capacitor Csub a pulse that determines a quantum charge Qc subtraction to the integrator. In parallel, the PG sends an increment or a decrement signal to the counter. This behavior permits a dead-time-free read-out.

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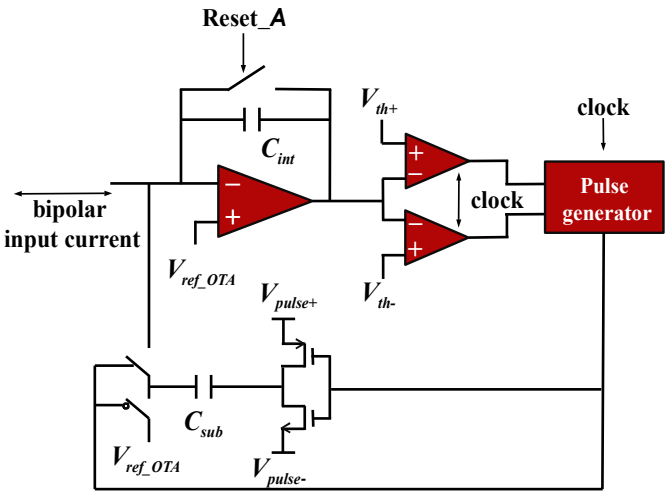

Fig 1: Schematic of a TERA09 channel.

The total charge read-out from the detector is given by the number of pulses generated during the measurement time multiplied by the value of the charge quantum Qc. The relationship between output frequency and input current, Iin, is therefore

$$v = Iin/Qc \qquad (1)$$

The charge quantum defines the sensitivity of the channel and can be varied by setting the two voltages Vpulse+ and Vpulse- as shown in the figure:

$$Qc = Csub\ (Vpulse+ - Vpulse-) \qquad (2)$$

The charge quantum is generated by sending a voltage pulse on the top plate of Csub, as shown in Fig. 3. The capacitor generates two δ-like current pulses of equal absolute value and opposite polarity. One pulse is used to subtract the charge quantum from the input, while the other is discharged toward the OTA reference voltage. Such selection is made by delaying the same pulse used to generate the current pulses and using it to control two CMOS switches. The resulting waveforms are shown in Fig. 4.

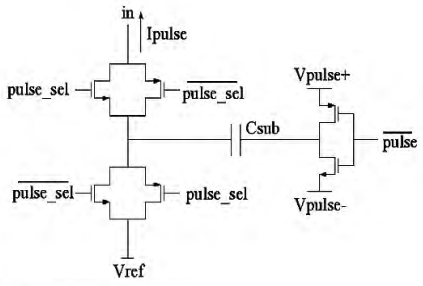

Fig 3: Charge subtraction circuit.

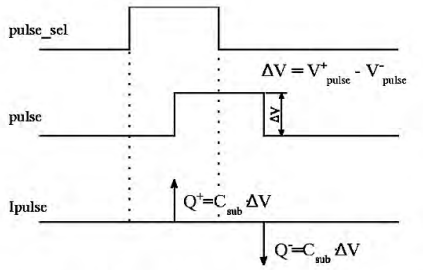

Fig 4: Charge subtraction waveforms.

It should be noted that the voltage across the switches is always equal to the OTA reference.

Another factor limiting the resolution of the circuit is the charge injected by the parasitic capacitors of the switches in the subtraction circuit. This charge is partially compensated by the use of CMOS switches and is minimized by choosing minimum size transistors.

Such a channel architecture, coupled with an up/down synchronous counter, can accept input currents of both polarities. This allows a better control of the pedestal offsets having the possibility to precisely detect and correct for the leakage currents.

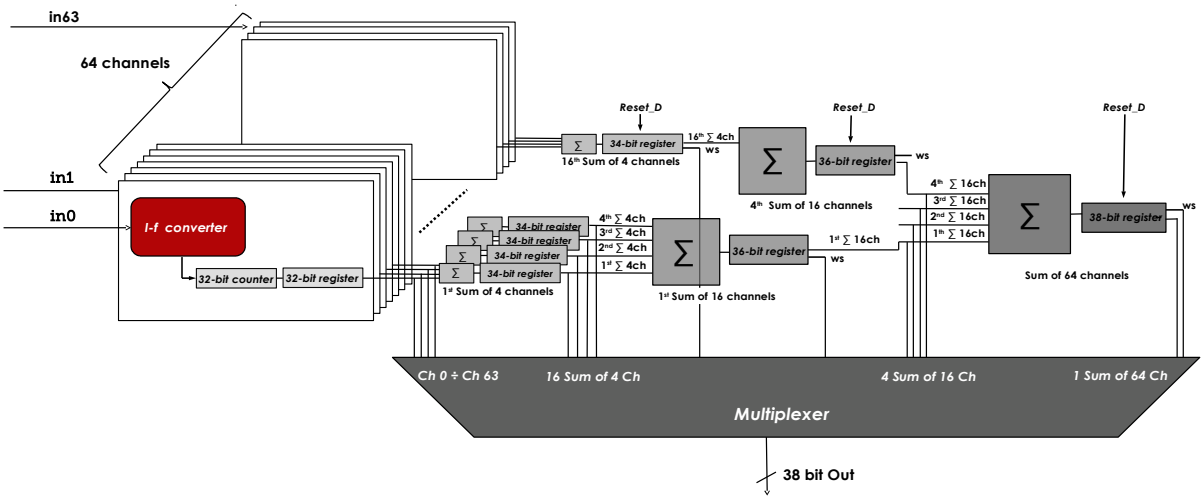

Fig. 2: The overall schematic of the TERA09 chip

The integration capacitor of all channels can be discharged via a common digital input Reset_A. Similarly, all counters can be zeroed via a common asynchronous digital input, Reset_D. The read-out of the counters can be done independently with respect to any other operation.

The channel is clocked by a 250 MHz master clock. A Moore-style finite state machine (FSM) provides the counter input signals as well as the feedback signals for the charge subtraction. The maximum conversion frequency is 1/4 of the master clock frequency, i.e. 62.5 MHz.

B. The pulse count and sum logic

Fig.2 represents the chip architecture. Through an external latch signal, the counters contents of all the channels are simultaneously loaded in 32 bits registers. An integrated system of adders provides the sum of groups of 4, 16 and 64 channels. These values are stored in additional registers. The registers can be addressed and read out through a multiplexer. An extension of the dynamic range can be obtained by connecting together a group of input channels to the same input. In this case, the current is split among several channels, thus avoiding saturation, and can be accessed by addressing the register containing the corresponding sum. Each register also provides an output warning signal (ws) that is activated whenever the most important bit of the counter switches from 0 to 1. A logic OR of all the warning signals alerts the user that an overflow situation is approaching.

III. Experimental setup

The experimental setup used to characterize the ASICs is based on a National Instrument PXI chassis with a 7813R FGPA, interfaced to the host PC using the LabVIEW for FPGA software [10,11].

The TERA09 design (chip size 4.68 x 5.8 mm^2) has been produced in a CMOS 0.35 µm AMS technology, in a Multi Project Wafer organized by Europractice [12]. The chips are encapsulated in an MQFP 160 package and mounted on a socket that is housed on the TERA09_Testboard. This test board, adapting the TTL logic to the CMOS one (and vice versa), receives controls and addresses sent from the FPGA to the chip and gives back the chip outputs.

For most of the tests we need to inject a precise constant current into a given channel or a current equally distributed over all the 64 channels, in a parallel interconnection. For this reason, we chose a Keithley 2400 source meter in the voltage source configuration that has been connected to the chip input via a large resistor (10 MΩ in the case of single channel charge injection or 1/10 MΩ, for the parallel of 64 channels, each one with a 10 MΩ inductance). The Keithley 2400 provides a precise voltage source in the range between 1 mV and 211 V, which corresponds to a current from 100 pA to 21 mA with a 0.012% accuracy. For higher currents, we used a Bertan 323 model HV power supply (which provides a voltage source up to 3kV). At this point we don't have a single source that covers with enough precision the 6 orders of range needed, but the relative error on the measured current has been maintained the same.

IV. Test results

Forty prototypes of TERA09 have been delivered and their characterization is still ongoing. In this section of the paper, we report some test results in order to assess the chip features. For these measurements two parameters have been set: 200 fC as charge quantum (typical value adopted in therapy) and a 250 MHz clock. With such a clock frequency, a maximum counter increment frequency of 62.5 MHz can be achieved. Fig.5 shows the counter frequency as a function of the input current for a representative channel. A conversion linear region is present up to the saturation current of ± 12 µA, as expected considering (1). In order to evaluate the deviation from linearity we adopted two different fits, separating the positive and the negative currents. Results are reported in Fig. 6.

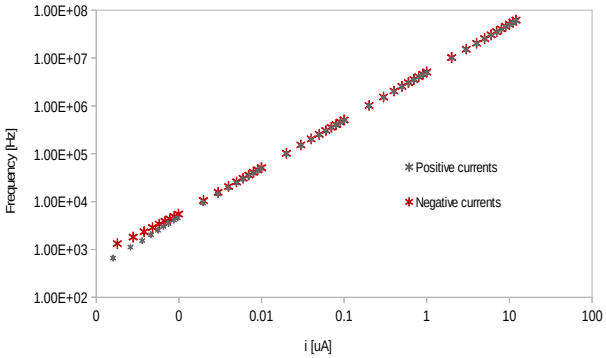

Fig. 5: Frequency as a function of the input current, for a single channel, in a 250MHz clock and 200fC of charge quantum configuration.

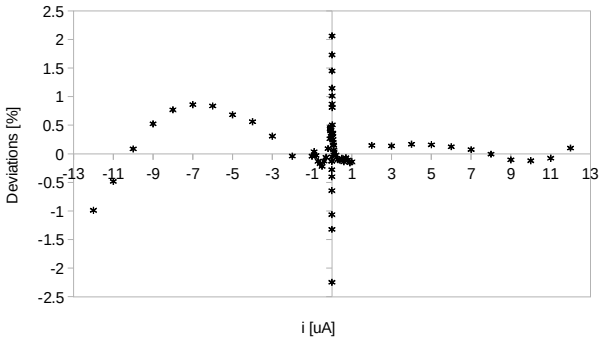

Fig. 6: Linearity deviations based on two different linear fits, respectively for positive and negative currents, for a single channel, in a 250MHz clock and 200fC of charge quantum configuration.

As explained in the section II B, the ASIC input current range can be extended with a parallel interconnection of channels. Therefore the declared maximum range is reached interconnecting all the channels. The linearity and deviations from linearity results, for the sum of 64 channels, are reported in Fig. 7 and Fig. 8.

Another important validation step is the charge resolution uniformity check. As previously reported, the charge quantum is our conversion factor and one of the design goals of this ASIC is having 64 parallel channels as uniform as possible.

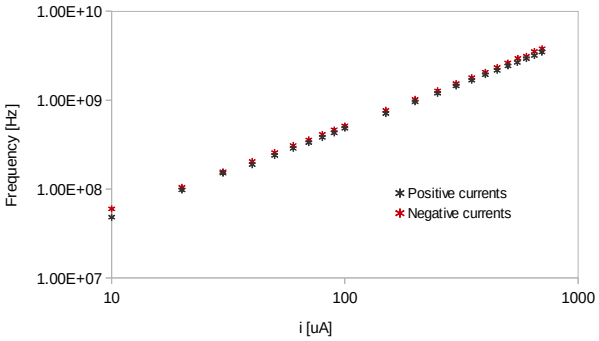

Fig. 7: Frequency as a function of the input current, for 64 channels interconnected in parallel, in a 250MHz clock and 200fC of charge quantum configuration.

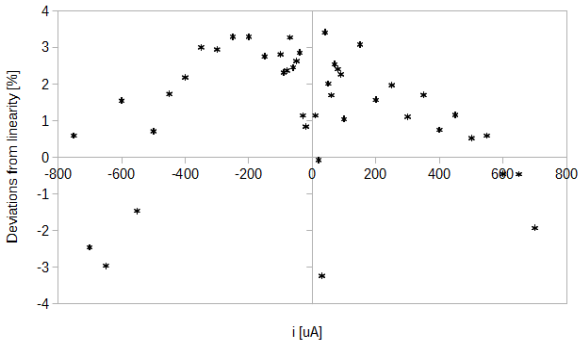

Fig. 8: Linearity deviations based on two different linear fits, respectively for positive and negative currents, for 64 channels interconnected in parallel, in a 250MHz clock and 200fC of charge quantum configuration.

Fig. 9 shows the variation of the charge quantum changing the ASIC channel. This distribution is a representation of the gain spread of the converter, obtained by injecting 1 µA current to each channel. Another test carried out for the channels gain uniformity is the one represented in Fig.10. In that case a 10 µA current was injected into a simple fan-in board that subdivides the input in 64 outputs through 64 10-MOhms surface-mounted resistors. This method is the base for the range extension that will be used with the detectors.

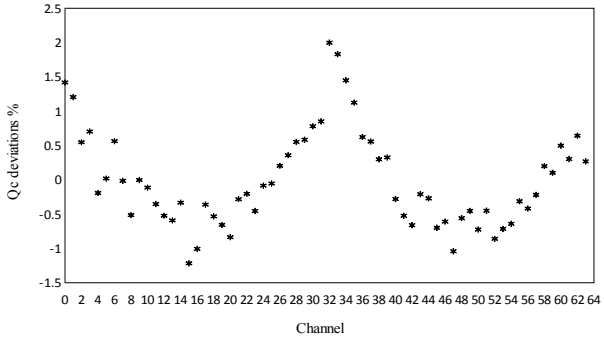

Fig. 9: Charge quantum deviations for the different channels, obtained from 1uA input current measurements.

The PCB test board has two input connectors each corresponding to a set of 32 channels of the ASIC. The trend of the deviations in Fig. 9 and Fig. 10, match the pinout (the pin are placed in a consecutive order) in the sense that for the external pins (1,2,3.. and 30,31,32) we obtain similar results that are different from the central region.

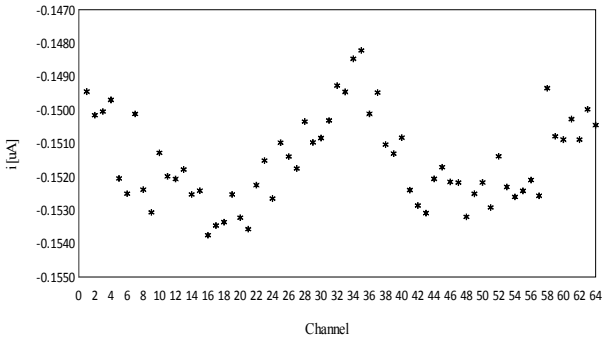

Fig. 10: Distribution of a 10uA input current, equally shared among the entire set of ASIC channels.

CONCLUSIONS

The improvements in particle therapy need to be followed by instrumentation upgrades. In this paper we present a new front-end, read-out ASIC designed to deal with the new and the future gas detectors for high intensity ion beams. The relative channel-to-channel gain, the quantum charge spreading and therefore the conversion linearity deviations are in the order of 1-3 %, as requested in medical applications.

ACKNOWLEDGMENTS

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[11] Information about the product can be found at the National Instruments web page /http://www.ni.com/labview.

[12] Information about the product can be found at the Europractice web page /http://www.te.rl.ac.uk/europractice_com.