A single ion discriminator ASIC prototype for particle therapy applications

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Abstract

In the framework of the development of future advanced treatment modalities in charged particle therapy, the use of silicon sensors is an appealing alternative to gas ionization chambers commonly used for beam monitoring. A prototype of a device, based on Low-Gain Avalanche Diode (LGAD) sensors with 50 μm thickness, is being developed to discriminate and count single beam particles. This paper describes the design and characterization of ABACUS, an innovative multi-channel ASIC prototype for LGAD readout, based on a fast amplifier with self-reset capabilities. The design goals aim at detecting charge pulses in a wide range, from 4 fC to 150 fC, up to 70 MHz instantaneous rates, with a dead time of about 10 ns or less and efficiency larger than 98%. The characterization results indicate that even at the lowest input charge the signal-to-noise ratio is 15, high enough to keep full efficiency and preventing fake counts from the electronics noise. The dead time was found to be in the range between 5 ns and 10 ns, allowing to reach a full counting efficiency up to instantaneous rates of 70 MHz or larger, depending on the input charge.

Keywords: Single ion detectors, Particle therapy, ASIC design, Silicon sensors.

1. Introduction

The Italian National Institute for Nuclear Physics (INFN) and the University of Torino are developing an innovative device for single ion discrimination and counting based on thin silicon detectors readout by fully custom electronics, to monitor the beam flux in proton therapy. This task is part of the INFN R&D project MoVeIT [1], an interdisciplinary collaboration involving various national research groups and the three Italian particle therapy facilities (CNAO [2], LNS [3], TIFPA [4]). MoVeIT aims at developing innovative treatment planning systems and new verification tools in radiobiology to tackle the new horizons in particle therapy, and, within this framework, the research of innovative detectors originates from the limits that the current instrumentation poses to future dose delivery strategies [5]. Indeed, the sensitivity of ionization chambers (ICs), the state-of-the-art beam monitors in charged particle therapy, limits the minimum number of particles that can be safely delivered to the order of thousands per spot, while their slow collection time (hundreds of microseconds) precludes the use of ICs on fast beam delivery strategies like, for example, volumetric rescanning and line scanning [6] to mitigate interplay effects between beam and organ motion [7]. To overcome these drawbacks, the project aims at exploring the use of thin silicon sensors (50 μm) based on the Low Gain Avalanche Diode (LGAD) design [8] with an internal gain of 10-15, achieved through a thin p+ layer implanted just beneath the n++ electrode. The signal extracted from these sensors has a well-defined shape, which amplitude is directly proportional to the internal gain, and its time duration (i.e. the charge collection time) is directly proportional to the sensor active thickness. A typical 50 μm thick LGAD has a charge collection time of about 1.5 ns, allowing single ion discrimination at clinical rate, and therefore well-suited to develop a particle counter for real-time beam monitoring. Moreover, to reduce the range uncertainties in particle therapy, several techniques and devices are being developed for in-vivo range verification [9] and most of them will take great advantage by the single ion discrimination capability [10].

As a proof of concept, a prototype is being developed in order to count the number of ions in an active area of 3x3 cm^2 within 2% accuracy for radio biological instantaneous fluence rates up to 10^8 $cm^{-2}s^{-1}$ and to measure the beam profile with a spatial resolution related to the detector segmentation (i.e. a spatial resolution of $\sim$50 μm for $\sim$80 μm wide and $\sim$150 μm pitch sensors).

Dedicated LGAD sensors segmented in strips and with an active thickness of 50 μm have been developed and produced by Fondazione Bruno Kessler (FBK, Trento) for this application. These sensors of area 2 mm^2 (5pF equivalent capacitance) are designed to operate at an expected average rate per channel up to 2 MHz. Assuming a random time distribution of the particle arrival and a paralyzable model of inefficiency effects due to signal overlapping [11], the required accuracy can be achieved discriminating signals with a maximum front-end dead time of 10 ns,corresponding to a discrimination frequency up to 100 MHz for regular pulses. For a synchrotron providing a beam with a bunch structure, the design specifications refer to the average beam flux inside each bunch. In a cyclotron the maximum dead time of the system is constrained by the particle delivery, which is synchronous with the phase of the radio-frequency with a typical period of about 10 ns. Based on [12], [13], Geant4

simulations of energy deposit in the sensor were performed for clinical proton and carbon energies energies respectively from 60 MeV to 250 MeV and from 120 MeV/u to 400 MeV/u. This simulation results indicates that, in order to meet the required accuracy, the electronics should be efficient in detecting pulses with range of charges between 4 fC and 150 fC (adopting sensors with gain factor 1, in case of Carbon ions).
This paper reports on the design and the characterization of a custom front-end electronics for silicon sensors in particle therapy application. Aiming the single ion detection at clinical particle rates, the electronics requirements include nanosecond-level shaping time and high input dynamic range in charge. Concerning the use of LGAD and ABACUS with heavier ions, the energy released in the sensor would be so large ($\sim Z^2$) that no internal gain would be needed to discriminate the ions while the expected lower beam flux would somehow relax the maximum counting rate requirements.

2. Design of the front-end circuit

Prior to start with a new ASIC development project, a state-of-the-art analysis was performed. Considering the field of application, beam monitoring in particle therapy is currently based on gas ionization chambers, where the advanced readout electronics is optimized for high intensity fluences [14]. Nevertheless, due to the detector features, those ASIC architectures are intended to manage average currents as input signals, without the possibility to detect the charged released by single ion interaction. In this sense, solid state detectors have several advantages in terms of speed, sensitivity and charge resolution with respect to the gas detectors. An example of nanosecond-level shaping time front-end ASIC for silicon detectors is described in [15]; although this chip is promising fast and deals with a few pF sensors, this design is tailored for SiPM readout with a ∼30 fC expected minimum charge. A few custom front-end chips for timing applications [16], [17], have been developed to readout LGADs with design and features similar to the ones adopted in the project described in this paper. Although the proper sensor-ASIC matching, these front-ends show a shaping time which is not fast enough to cope with the input signal rate expected in the application here studied. In order to deal with a dead time below 10 ns and a wide charge input range, a new custom VLSI electronics has been developed. This circuit is integrated in a 24-channels chip, nicknamed ABACUS (Asynchronous-logic-Based Analog Counter for Ultra fast Silicon strips). In order to meet the requirements, the amplifier has been designed to provide signal shaping with a few nanoseconds time duration. The design choice is based on the use of a low noise Trans-Impedance Amplifier (TIA) effective in providing signals with short rise time and on a feedback-reset circuitry used for a fast return to baseline once the input signal has been detected. Figure 1 depicts the chip layout top view. The lower part of the ASIC integrates the input pads which are packaged between grounds to better isolate the channel inputs, while the driver outputs are placed in the upper part. On the shorter edges the bias currents and the bias voltages are placed as well as the control signals. The 24 channels are symmetrically separated into two main sectors, with a central region filled with filtering capacitors.

The ABACUS area is 2x5 mm^2 and it has been designed with a commercial 110 nm

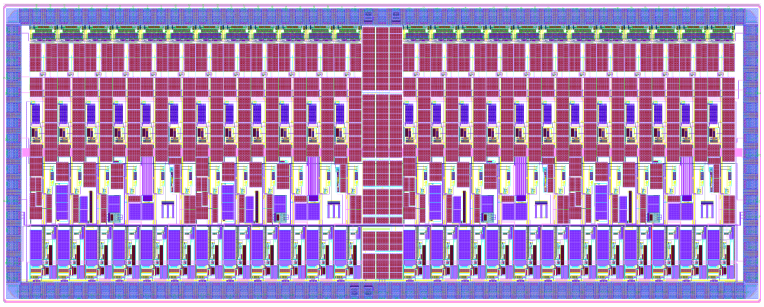

Figure 1: ABACUS layout top view. The ASIC pad-frame consists in 140 pads with 24 inputs and 48 differential outputs placed on the lower and upper long edges respectively, whereas the lateral pads are dedicated to bias and controls.

MOSFET technology node. The ASIC top level is arranged in four sectors with six channels each and a sector-level bias cell, mirrored on the chip edges to mitigate possible gradients responsible for channel-to-channel inhomogeneities. The chip will be positioned aside of the 3x3 cm^2 sensor at approximately 1 cm distance and will never be directly exposed to the primary pencil beam. Considering that no digital logic is implemented, data corruption induced by single events from scattered radiation is not a concern for this application. Additionally, the 110 nm CMOS technology has been proven to be tolerant to ionizing radiation up to a total dose of 50 kGy [18]. Considering an average dose of 2 Gy delivered to a patient, 100 patients per day, 250 working days per year and assuming a very pessimistic estimate of 10% of dose delivered to the ASIC, the chip would show no degradation due to radiation for several years.

Sixty ABACUS ASICs have been taped out in an Europractice multi-project wafer. The next subsection reports the functional level description of the ASIC channel and two dedicated subsections provide insights into the amplifier and the feedback-reset blocks.

2.1. ABACUS channel

A block diagram of one ABACUS channel is shown in Figure 2. The channel can be divided into four parts, according to their role: amplification (blocks 1 and 2), discrimination (blocks 3 and 4), driver (blocks 5 and 6) and feedback reset (blocks 7 and 8). Standard digital buffers have been included for signal shaping both for the long metal nets connecting the driver and to achieve a sharp reset signal acting on the amplifier feedback capacitor (block 9).

The amplifier is a TIA-based design which shapes its output signal with a fast rising edge ($\sim$ 1.6 ns) while the falling edge has a long tail, depending on the product C_f R_f $\sim$ 18 ns. Once amplified, the signal is sent to a two stages leading-edge discriminator where it is compared with an external threshold. The pulse generated by a signal over threshold activates a feedback reset circuitry designed for a fast return to the baseline to prevent front-end from saturation. At the same time, the discriminator output signal is propagated off-chip through a Current Mode Logic (CML) differential driver with a 50 Ω internal termination, selected to achieve high speed while keeping a 1.2 V common voltage supply for the entire chip.

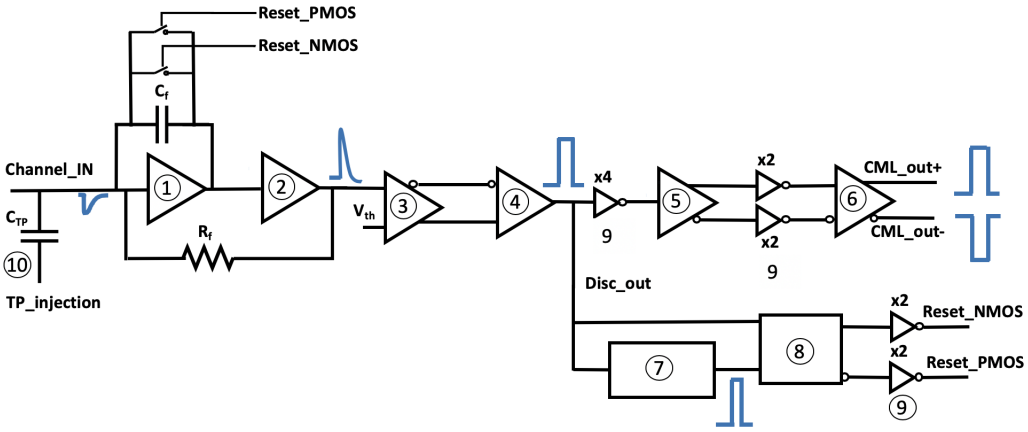

Figure 2: Block diagram of the ABACUS channel

. Charge sensitive amplifier (1), low-pass filter (2), leading edge discriminator (3,4), single ended to differential converter (5), current mode logic driver (6), pulser (7), recovery (8), inverters for signal shaping (9), test pulse circuit (10).

The ASIC has two integrated circuits for test-pulse injection, one connecting the even and one the odd channels, allowing to feed an externally generated pulse through a 40 fF test pulse capacitor (C_{TP}).

2.2. The amplifier block

Figure 3 represents the block diagram of the ABACUS amplifier. The resistor feedback R_f is used to implement the TIA configuration in a two stages amplifier, where the first block is based on a Charge Sensitive Amplifier (CSA) and the second one, an active non-inverting low-pass filter, consists in a Operational Trans-impedance Amplifier (OTA). The CSA has been designed implementing low noise techniques similar to other front-end amplifiers developed for timing applications with LGADs [16].

The amplifier transfer function can be expressed as follows:

$$T(s) = \frac{R_f}{(1 + s\tau_r)(1 + s\tau_f)} \tag{1}$$

where the time constants for the TIA output voltage rising (τ_r) and falling (τ_f) edges can be written as:

$$\tau_r \approx \frac{C_{det} \cdot (C_f + C_l)}{C_f g_{m1}} \tag{2}$$

and

$$\tau_f \approx \frac{C_f \cdot R_f}{(1 + R_2/R_1)} \tag{3}$$

In Equations 2 and 3 C_{det} is the detector capacitance, C_f is the CSA feedback capacitance,

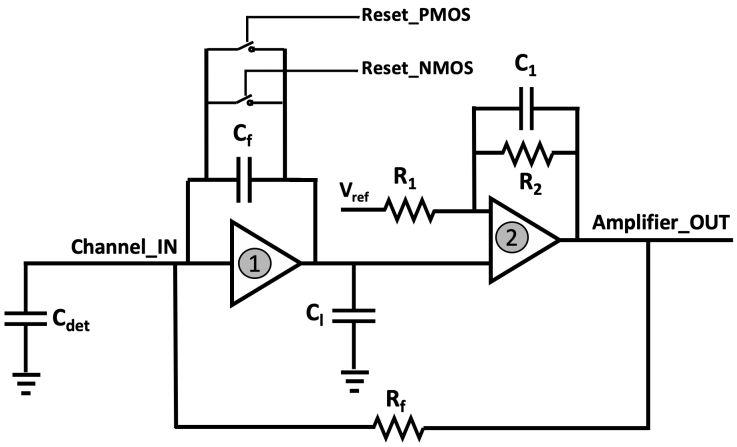

Figure 3: Block diagram representation of the ABACUS amplifier. A CSA (1) is followed by a low-pass filter (2), consisting in a OTA.

C_l is the equivalent capacitance of the CSA load, g_{m1} is the transconductance of the CSA input transistor, $(1 + R_2/R_1)$ is the voltage divider at the filter input, V_{ref} is a reference voltage used to adjust the filter operating point.
As reported in Equation 2, in order to compensate for the detector capacitance (5 pF), g_{m1} must be large. In addition, large C_f was chosen in order to ignore the contribution of C_l. To meet these requirements, a large bias current of ∼8 mA and a feedback capacitance of 500 fF have been set for the CSA. The R_2/R_1 ratio has been chosen larger than 1 to achieve additional gain. For the feedback resistance R_f, a value of 35 kΩ has been chosen in order to keep the noise low, provide a sufficient low-frequencies gain, while contributing for the signal shaping and for the amplifier stability. The amplifier output amplitude depends on the effects of both the CSA and the filter. Operating on V_{ref}, it is possible to use the filter to attenuate the signal for measurements of a wide range of input charges. Although from simulation the conversion factor can be adjusted up to 2.5 mV/fC, the nominal setting is obtained with the filter gain at ∼1, resulting in a 1.21 mV/fC overall conversion factor. Figure 4 shows the amplifier output amplitude as a function of the input charge, in the nominal operating condition. The amplifier behaves linearly up to 120 fC, where it starts saturating. From transient noise simulations, the expected rms noise of the entire amplifier is found to be 0.47 mV.

2.2.1. The Charge Sensitive Amplifier

The adopted LGADs provide negative currents and this lead to the choice of a single polarity front-end design. An additional reason for choosing single polarity stages is related to a better noise figure, improving the discrimination efficiency at high rates and low charges. In Figure 5 the transistor-level schematic representation of the ABACUS CSA is shown. The CSA topology consists of a NMOS input telescopic cascode with two independent branches.

The open loop gain is given by the product between the NM1 transconductance and the drain-source resistance of the cascoding device. A second independent branch is used

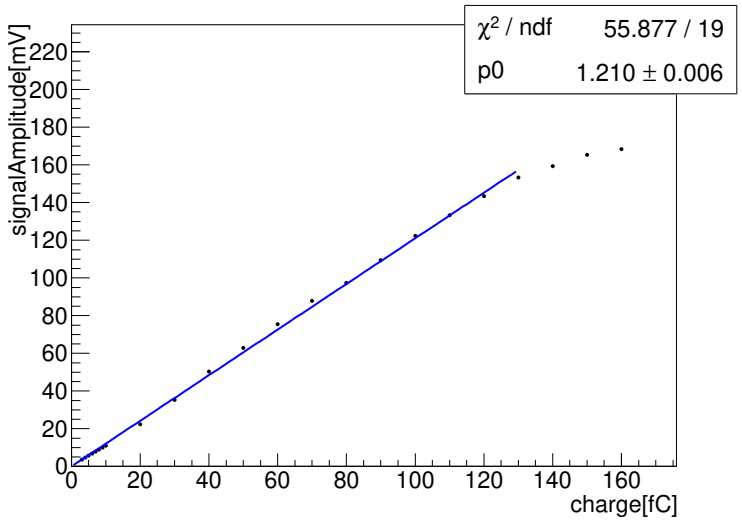

Figure 4: Amplifier linearity simulation results. $p0$ is the fit slope, representing the charge-to-signal-amplitude conversion factor.

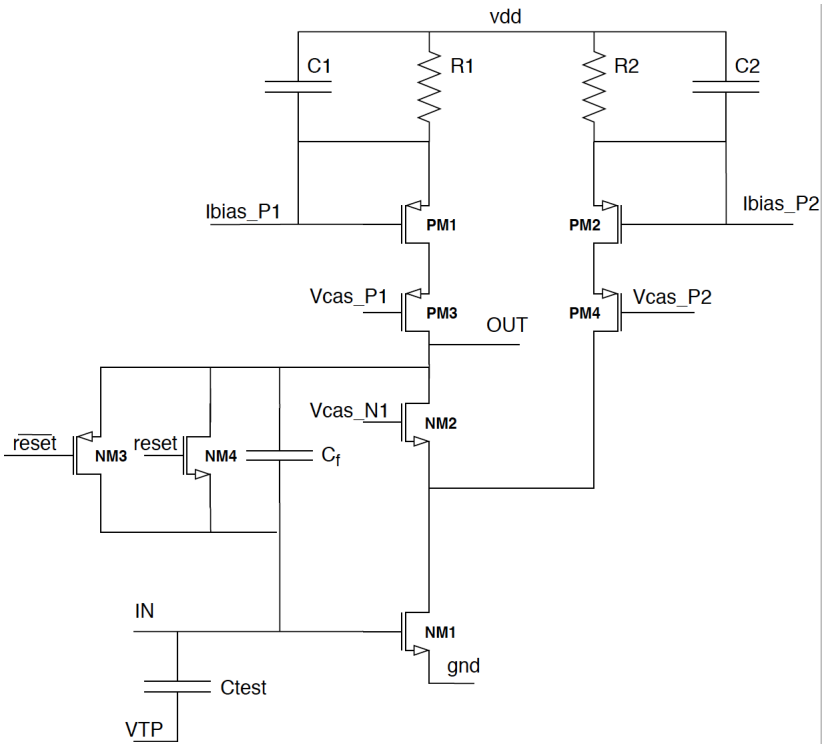

Figure 5: Schematic representation of the ABACUS charge sensitive amplifier.

to increase the open-loop gain. The left branch biases the cascodes PM3 and NM2 with $\sim 200\mu$A current; increasing this current, the output voltage slew rate increases but at the same time the swing decreases. The second branch of the CSA (transistors PM2 and PM4)

is used to provide to the input transistor the largest part of its current (∼8 mA).

2.3. The feedback-reset circuitry

The feedback reset occurs at channel level and each channel operates on his own capacitor, activating and managing this functionality independently from the others. The amplifier RC components in the feedback connection would result in a long tail that would limit the efficiency at large repetition rates. This effect has been mitigated by using the feedback-reset circuitry, which includes the sequential action of a pulse generator and a recovery system to activate the switching capacitor MOSFETs and reset the CSA feedback capacitor.

2.3.1. Pulse generator

The CSA feedback capacitor reset is performed by a block called "pulser". Referring to Figure 6, the discriminator output is inverted (line S1) and then is inverted again using a starved inverter to introduce a delay (line S2); finally a third inverter digitizes again the delayed signal (delayed_IN). This delayed signal is fed into a boolean AND gate with the original discriminator output. This allows to have a pulse that starts as close as possible in time to the discriminator output (1.2 ns, independently of the signal amplitude), lasting for a short time set by the RC delays of the inverters. Moreover, it is possible to change the pulse duration from a minimum of 0.4 ns to a maximum of 2 ns, operating with two bias voltages controlling the second inverter delay (PulserVbiasP, PulserVbiasN).

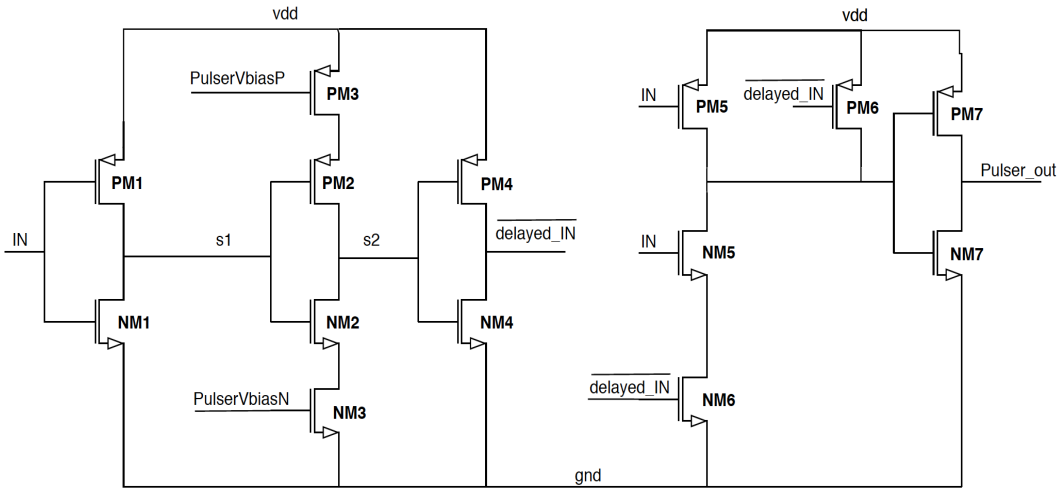

Figure 6: Pulser: transistor level representation. The output signal results form a boolean AND between the input and a delayed and inverted copy of the input. The two signals overlapping duration can be varied with the PulserVbiasP and PulserVbiasN voltages.

2.3.2. Recovery system

The Pulser action is designed to reset as fast as possible the amplifier output voltage to the baseline with the minimum possible deadtime. However, in situations characterized by high signal rates, the duration of the reset signal of the pulser could not be long enough

to bring the front-end signal below threshold, leading to the discriminator remaining fixed in a stuck condition. To avoid this effect, a circuit named "recovery" has been added. The recovery output signal is used to control an NMOS switch-reset transistor for resetting the amplifier feedback, whereas its negated signal is used to control a PMOS switch reset transistor adopted for the collection of the charge injection due to the NMOS switching. The working principle of the recovery block is based on a boolean OR between the pulser output and the discriminator output signals, the latter overtaking a high-pass filter with time constant $\tau = 3.5$ ns. In normal conditions the discriminator output is reset by the pulser signal well before τ. When the discriminator output is still high after τ, the recovery circuit generates a second longer reset pulse to the front-end which forces the restore of baseline.

3. ABACUS characterization

The ABACUS ASIC has been tested in laboratory to check its performance in terms of electronics noise, amplifier baseline stability and gain. The ASIC measured power consumption is $\sim$30 mW/ch and the main part of this power is equally shared between the amplifier and the driver. It is worth to mention that the power budget was not a design constraint whereas the single ion discrimination capability over a wide charge and frequency range is the ABACUS figure of merit. This point has been stressed during the tests.

3.1. Setup and methodology

A custom board for testing the ASIC has been developed integrating trimmers for currents and voltages settings, as well as a 16-bits DAC for remote setting of the discriminator threshold voltage. An FPGA was used to readout and control the ASIC, while the input signal has been provided by means of a voltage pulse source connected to the channel input through a capacitor. Two variants of this setup have been used, one based on the integrated test pulse circuit and a second one using an external capacitor connected to the input pad of a single channel. For the setup based on the integrated capacitors, the pulse injection has been provided using an external pulser unit Active Technologies Pulse Rider PG-1072). In Figure 7, an oscilloscope screen-shot shows one polarity of the output differential signal (CML_out+) and the input form the pulser (Pulse_A), for 33 fC charge pulses with 125 MHz repetition rate. The delay between the falling edge of the pulser signal and the ASIC output pulse is $\sim$5 - 6 ns, for a 33 fC injected charge, and is due to the intrinsic delays of the amplifier and the discriminator blocks and to the R-C contributions from layout parasitic effects.

This configuration has the intrinsic limitation in the maximum injected charge of 48 fC, due to the maximum voltage of 1.2 V that can be injected through the 40 fF internal capacitance. Furthermore, for each voltage pulse two input charges of opposite polarities are injected into the channel. Since the reset circuit is not activated with a positive input charge, this would lead to a drift of the baseline especially at large input frequencies. A second setup based on a 500 fF external capacitor and uni-polar voltage input steps has been used. An external board (LTC200IY-2303A) based on a 16-bit high speed DAC with

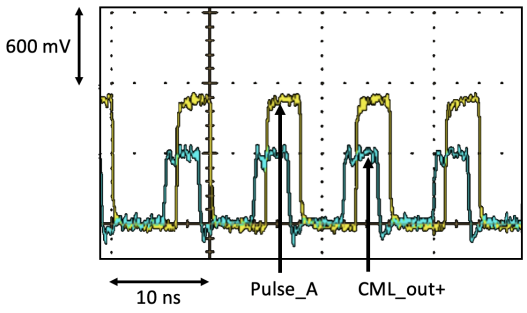

Figure 7: Oscilloscope screenshot with pulser-injected input signal (yellow) and the CML driver output signal (light blue), corresponding to a 33 fC injected charge and pulse frequency of 125 MHz. The driver output results from the falling edge of the injected pulse.

300 mV voltage swing and 2.2 GHz bandwidth was implemented to provide a voltage ramp with programmable step height and frequency. A LabVIEW control program was used to configure the ramp cycle selecting the number of steps, their duration and the ramp plateau width. In order to avoid instabilities of the amplifier, a slow falling ramp was implemented using small voltage steps. Figure 8 shows an oscilloscope screenshot with 10 voltage steps separated by 100 ns, together with the positive polarity output of ABACUS.

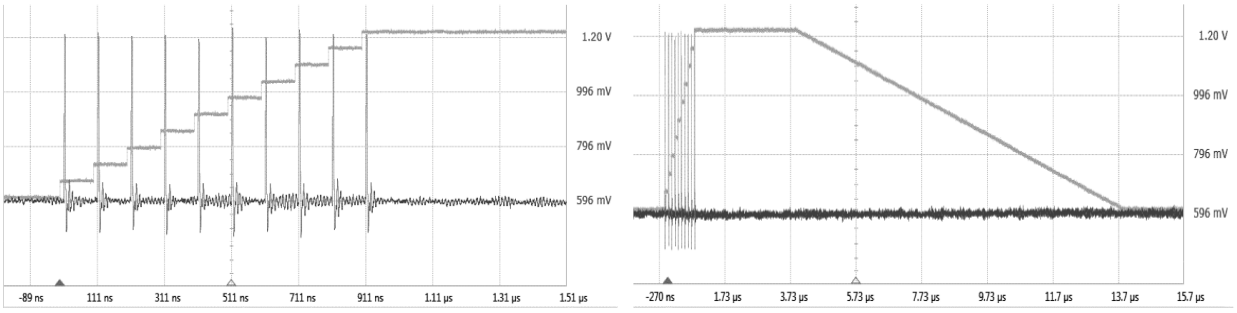

Figure 8: Left: 10 steps voltage ramp with a 100 ns step-separation and the ABACUS driver output signal (CML_out+). Right: the complete ramp cycle, composed by the voltage steps, the plateau and the slow falling tail.

In both setups, the ABACUS differential outputs have been readout by an FPGA board (Xilinx Kintex7-Ultrascale XCKU040), sampling the outputs at 1 GHz and counting the number of 0-1 transitions. The same FPGA has been used to control the discrimination threshold by operating the 16-bit on board DAC. A LabVIEW program was prepared to acquire the counting rate and to setup runs increasing the threshold in small steps during the acquisition. An example of results for 30 fC pulses injected at 10 MHz is shown in the left side of Figure 9; the counting efficiency, defined as the ratio of counting rate over the input pulse rate, is here shown as a function of the threshold. Similar runs were performed with different pulse frequencies up to 130 MHz for both the setups. More in detail, charges ranging between 3 fC and 20 fC where injected into the 40 fF integrated capacitor whereas the the external 500 fF test pulse capacitor was used for the 30 fC-160 fC range. Increasing

the threshold, the counting efficiency moves from large values around the baseline level, where the noise induces high frequency of counts, to a flat plateau where the signal is discriminated with full efficiency. When the threshold reaches the signal peak, the counting efficiency drops to 0, as shown in the right panel of Figure 9, with a slope caused by the electronics noise which overlaps with the signal.

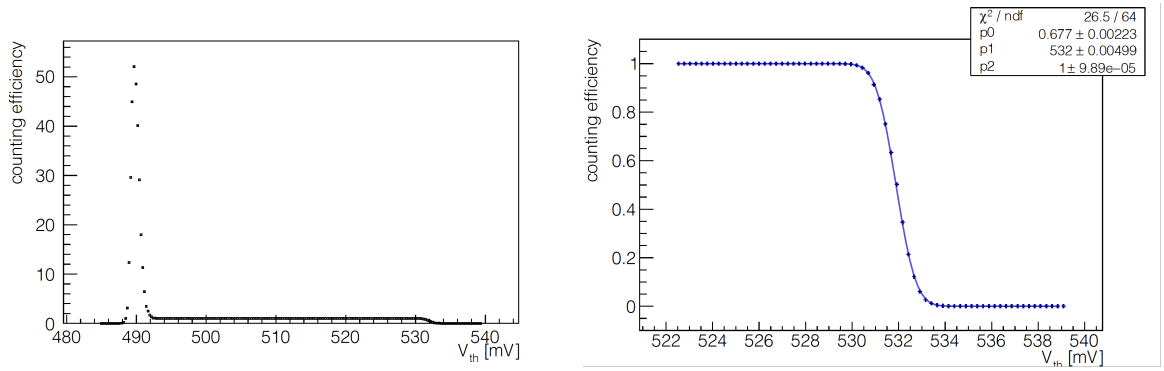

Figure 9: Left: example of a discriminator voltage threshold scan for a 30 fC signal injected into the chip test pulse pad with 10 MHz repetition rate.
Right: expanded view of the threshold axis, where the counting efficiency drops from 1 to 0. The p0 parameter represents the noise standard deviation expressed in mV whereas the p1 parameter is the voltage threshold at which the efficiency is equal to 0.5. The p2 fit parameter represents the efficiency normalization factor.

In order to fit the points, a convolution of a step function with a gaussian (sigmoid fit) has been used to extract the signal amplitude corresponding to the threshold voltage at 0.5 efficiency (p1 fit parameter) and the standard deviation of the electronic noise (p0 fit parameter):

$$f(x) = p_2 \int_x^{+\infty} 1/(\sqrt{2\pi p_0^2}) e^{-(x-p_1)/2{p_0}^2} dx' \tag{4}$$

where x is the voltage threshold and p_2 is a parameter adopted for data normalization.

3.2. Results

The amplitude of the amplifier output has been estimated with the threshold scan described before, as a function of the injected charge and pulse frequency. A configuration reproducing the conversion factor of Figure 4 has been adopted for this test. For small charges up to 20 fC the integrated 40 fF capacitor was used (Figure 10, left), while for large charges the pulses were injected into the external 500 fF capacitor to extend the charge range up to 160 fC (Figure 10, right).

In both the figures, the signal amplitudes measured with 1 MHz pulse frequency have been reported after the subtraction of the baseline value, defined as the linear fit intercept.

The measured conversion factor (the p0 parameter in Figure 10) for the setup based on the external capacitor is compatible with the expectation from the simulation results reported in Figure 4. The left plot of Figure 10 is related to the internal test capacitor and

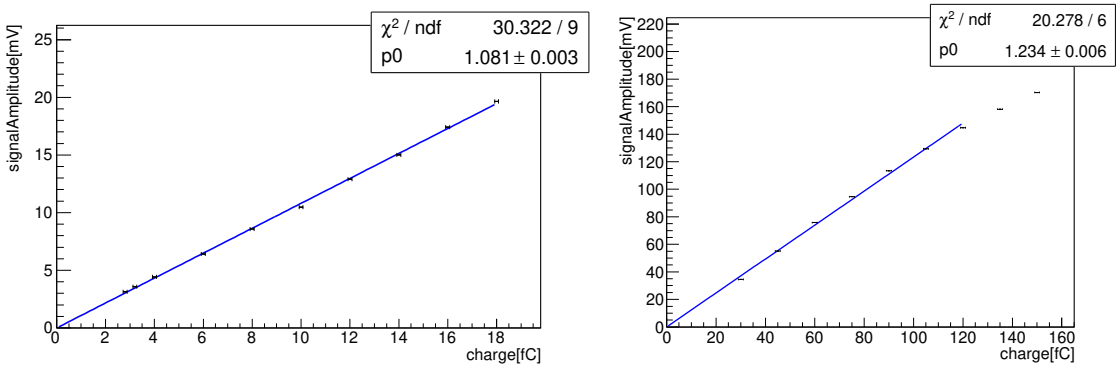

Figure 10: Amplitude of the amplifier output signal as a function of the charge injected at 1 MHz rate through the integrated 40 fF capacitor (left) or the external 500 fF capacitor (right).

the pulser-based setup; in this case the pulser rising time (τ_r) is fixed by the instrument constraints to 200 ps whereas the DAC-based setup has a 1 ns τ_r. Since the ABACUS amplifier has been designed with a bandwidth tailored to deal with LGADs with a typical charge collection time of 1 ns, faster signals result in lower amplification. For both the charge ranges the counting efficiency is 100% and the amplifier output is linear with the input charge, up to 120 fC where the amplifier saturation starts to occur.
Figure 11 shows the noise standard deviation determined by the sigmoid fit described earlier as a function of the charge injected at 1 MHz through the 40 fF internal capacitor (red markers) and through the 500 fF external capacitor (black markers).
The results indicate that the electronics noise is independent on the injected charge, for each set of measurements. The data collected operating with the integrated test capacitor are within $\pm$ 0.05 mV the electronics noise value obtained from circuit simulation (0.47 mV). This kind of shift is compatible with what was expected during the design phase, due to simulation approximations. The higher noise level measured using the external capacitor is related to parasitic effects due to the longer injection path. The test has been repeated at different repetition rates with no effect on the measured values.

In order to study the dead time of the discrimination circuitry, the efficiency in separating two consecutive input pulses is measured as a function of their time delay. The 2-pulses set repetition rate was fixed at 10 KHz in order to avoid the high-frequency continuous pulse effects, discussed afterwards as dedicated test results. The results are shown in Figure 12 for different input charges. A full 2-pulses detection efficiency is achieved with time delays greater than 10 ns while a drop in the efficiency appears at lower time delays depending on the input charge. Two different effects degrade the discrimination efficiency: for low charges, e.g. 6 fC, the signal-to-noise-ratio (SNR) is low and the discriminator could miss the signal detection whereas for very large charges, e.g. 100 or 150 fC, the amplifier return to baseline time is more affected by the larger signal amplitude. Therefore, the two effects are correlated because maximizing the SNR was not adopted as design solution since it would lead to either amplifier saturation or low discrimination frequency. The best result is achieved for 50 fC injected pulses.

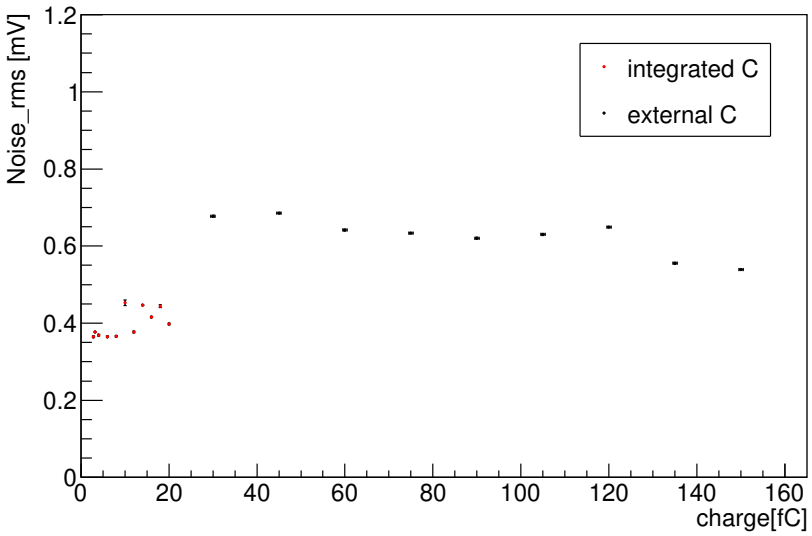

Figure 11: ABACUS noise standard deviation a function of the charge injected either into the 40 fF internal capacitance (red markers) or into the 500 fF external capacitance (black markers).

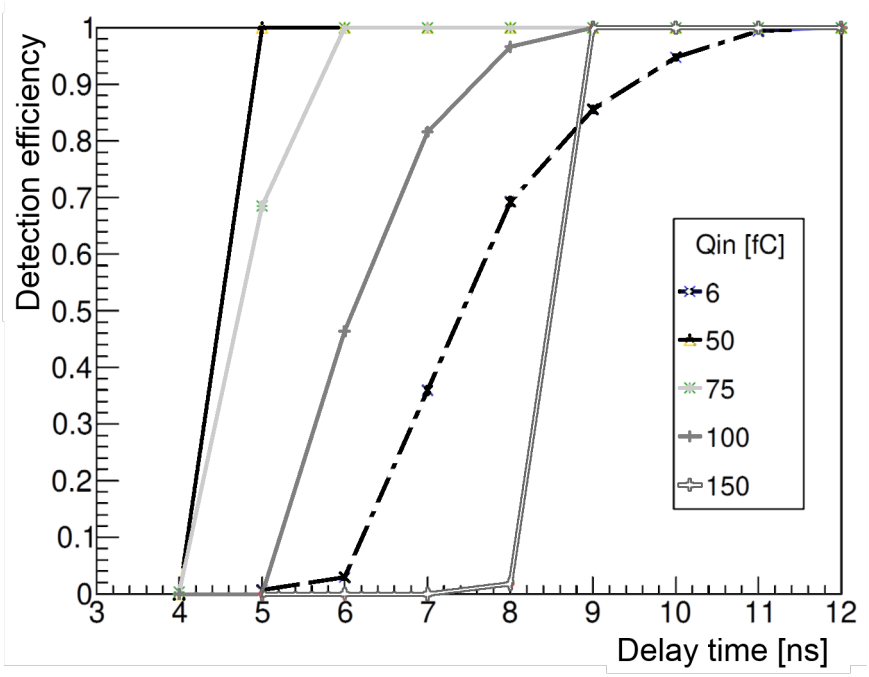

Figure 12: 2-pulse detection efficiency as a function of the time delay, for different injected charges.

The counting efficiency has been measured fixing both the input charge and the discriminator threshold while changing the signal repetition rate. This setup is based on the high speed DAC board, described in the previous section, providing configurable voltage ramps and

repeating the ramp cycle 100 times. Figure 13 reports the results for two injected charge pulses, 20 fC and 4 fC. For the 20 fC charge, increasing the signal repetition rate the counting efficiency remains higher than 99% up to 110 MHz, while for the lower charge the drop in efficiency starts at lower repetition rates. This behaviour is compatible with the higher dead time found at low charges.

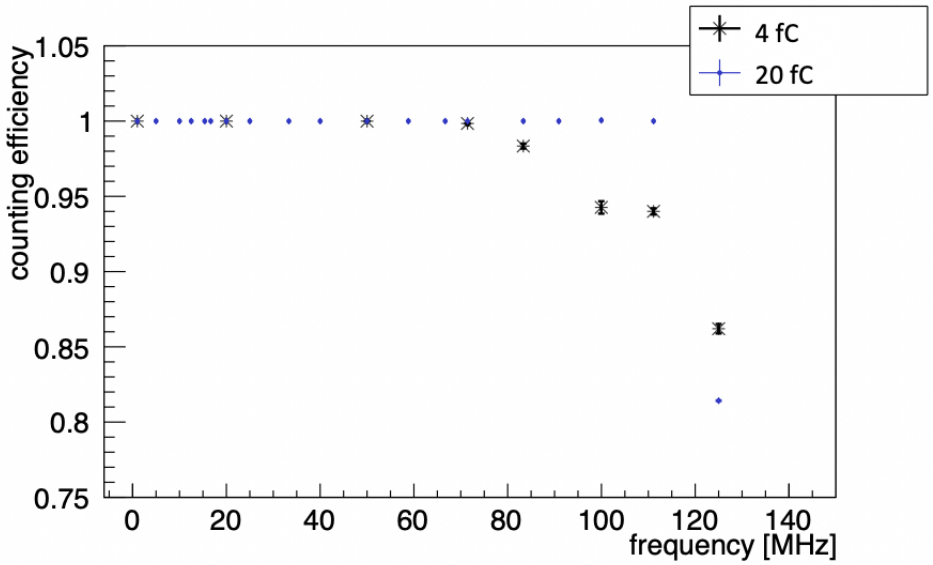

Figure 13: Counting efficiency vs frequency of the injected signal for 20 fC and 4 fC signal amplitudes. The signals are provided by the high speed DAC circuit board and the discriminator threshold has been fixed 3 mV above the electronics noise.

4. Discussion

The precise measurement of the delivered dose in particle therapy is a challenging task that relies on the precision and stability of the beam monitoring system. The reference detectors used since many decades are based on gas ionization chambers which offer several advantages in terms of simplicity, robustness, ease of operation and minimal perturbation of the beam. However, their sensitivity is limited to O(10^3) protons [19], while the charge collection time can be as large as hundreds of μs. These drawbacks prevent their use in emerging new dose delivery modalities aiming to mitigate uncertainties due to organ motion [7], like volumetric rescanning and line scanning [6], where faster beam movements and small doses need to be accurately monitored.

These drawbacks prevent their use in emerging new delivery modalities where faster beam movements and small doses need to be accurately monitored. As an alternative, solid state detectors offer sensitivity to single ions that could change the paradigm used for monitoring the beam flux from an integrated charge measurement to single ion counting. The direct measurement of the number of protons would not rely on accurate dosimetric

calibrations and on the beam particle energy. Recent developments of thin LGAD sensors allow to achieve very short signal duration with similar signal-to-noise ratio as traditional thicker silicon sensors. This, combined with fine sensor segmentation aimed to reduce the expected particle rate for each channel, would allow to count particles at the large fluxes of therapeutic beams.

The clinical constraint of counting efficiency better than 98% requires a very fast dedicated front-end readout able to detect pulses with the large range of charges expected for protons of different energies (from 60 to 250 MeV) in 50 μm silicon thickness. The minimum measured SNR of 15 demonstrates the capability of separating signals from the electronic noise even at the smallest input charge of 4 fC. Given the random time distribution of particle arrival, the overlap of signals is the limiting factor in the maximum achievable counting rate. Therefore, the dead time introduced by the electronics must be reduced as much as possible. The results obtained in terms of two pulse detection efficiency indicates that the dead time is always smaller than 10 ns for all the injected charges except for the 6 fC charge, where the detection efficiency is still larger than 95%. This effect is addressed to the fact that the low-charges are provided by the pulser with a pulse rising time not ideal for the ABACUS amplifier bandwidth, as explained discussing the 2-pulses detection efficiency results. Moreover, the low-charge discrimination is more affected by leakage or parasitics due to the fact that the pulse is not directly injected into the front-end amplifier but moves through the test pulse injection circuit, shared among several channels (all the even or all the odds channels).This result guarantees, with the current design of strip segmented LGADs, the measurement of a flux of 10^8 cm^{-2} s^{-1} with 2% accuracy for a beam provided by a cyclotron or for a continuous beam. Bunched beam from synchrotron of similar average flux could suffer for larger inefficiencies due to larger instantaneous particle rates in each bunch and would require smaller strip or pixel size.

5. Conclusions

A novel custom front-end ASIC for single ion detection in particle therapy applications has been developed. It integrates in a single chip 24 channels, designed with a trans-impedance amplifier followed by a discriminator with adjustable threshold. Particular care was devoted to the design of a fast baseline restore mechanism to achieve low dead time capability. A laboratory setup was prepared for the characterization which allows to inject pulses of different charges and frequencies. A FPGA-based readout system allows to count the pulses detected by the chip and to set values of the discriminator threshold. Threshold scans at fixed input charge and frequency were used to determine the amplitude of the amplifier output, as well as the noise. The results show good linearity of the amplifier for the range of charges expected for the envisaged application, with a gain compatible with the simulations. The low noise level, charge independent, lead to a signal-to-noise ratio larger than 10 even at the smallest input charges. The dead time was estimated by studying the efficiency in detecting two input pulses as a function of their time delay. The results indicate that a dead time smaller than 10 ns can be achieved for input charges larger than 6 fC. Finally, the fraction of detected pulses was measured as a function of the pulse rate, showing that

100% efficiency is achieved up to over 100 MHz for all the input charges but for 4 fC, where the efficiency starts to drop at 70 MHz. Therefore, the reported results demonstrate that the developed ASIC is compliant with the MoVeIT requests, as it is able to detect charge pulses in the range 4-150 fC up to 70 MHz instantaneous rate, with a dead time of about 10 ns or less and effiency larger than 98%.

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