The CGEM-IT readout chain

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ABSTRACT: An innovative Cylindrical Gas Electron Multiplier (CGEM) detector is under construction for the upgrade of the inner tracker of the BESIII experiment. A novel system has been worked out for the readout of the CGEM detector, including a new ASIC, dubbed TIGER -Torino Integrated GEM Electronics for Readout, designed for the amplification and digitization of the CGEM output signals. The data output by TIGER are collected and processed by a first FPGA-based module, GEM Read Out Card, in charge of configuration and control of the front-end ASICs. A second FPGA-based module, named GEM Data Concentrator, builds the trigger selected event packets containing the data and stores them via the main BESIII data acquisition system. The design of the electronics chain, including the power and signal distribution, will be presented together with its performance.

KEYWORDS: Micropattern gaseous detectors, front-end electronics for detector readout, detector control systems, data acquisition circuits, control and monitor systems online

Contents

1 Introduction

The Beijing Spectrometer (BESIII) is a high-energy physics experiment located at the Beijing Electron Positron Collider (BEPCII) [1]. BEPCII is a two-ring e^+ e^- collider, with a center of mass energy tunable between 2 and 4.9 GeV and a luminosity up to 10^{33} cm^{-2}s^{-1}. The cylindrical core of the BESIII detector consists of a helium-based (He-C_3H_8 60:40) multilayer drift chamber (MDC), as charged particle tracker, a plastic scintillator time-of-flight system, and a CsI(Tl) electromagnetic calorimeter (EMC), which are all enclosed in a superconducting solenoidal magnet providing a 1 T magnetic field. The solenoid is supported by an octagonal flux-return yoke with resistive plate counter muon identifier modules interleaved with steel. The acceptance of charged particles and gammas is 93 % over the 4π solid angle. The charged-particle momentum resolution at 1 GeV/c is 0.5 %, and the dE/dx resolution is 6 % for the electrons from Bhabha scattering. More details about the BESIII spectrometer are described in [2].

The BESIII experiment offers a unique setup to investigate charmonium and charmonium-like states, charmed mesons and baryons, light hadron spectroscopy, τ physics, QCD and CKM parameters, baryon form factors, and new physics by studying rare and forbidden decays [3].

The current tracker, consisting of an inner chamber and an outer chamber, has been taking data since 2009. Due to the high luminosity of the experiment, it is degrading with a gain loss per year of about 4 % for the innermost layers, as shown in figure 1 [4]. To partially compensate the gain loss, the voltage has been raised and about 0.2% water vapor was added to the MDC gas mixture to solve the cathode aging problem.

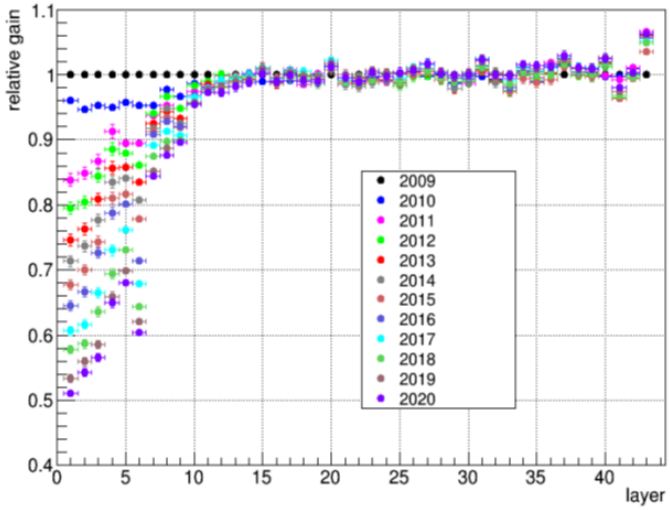

Figure 1: Gain loss of the MDC with respect to 2009. The inner MDC is composed of the eight innermost layers. Their gain loss per year is about 4 %.

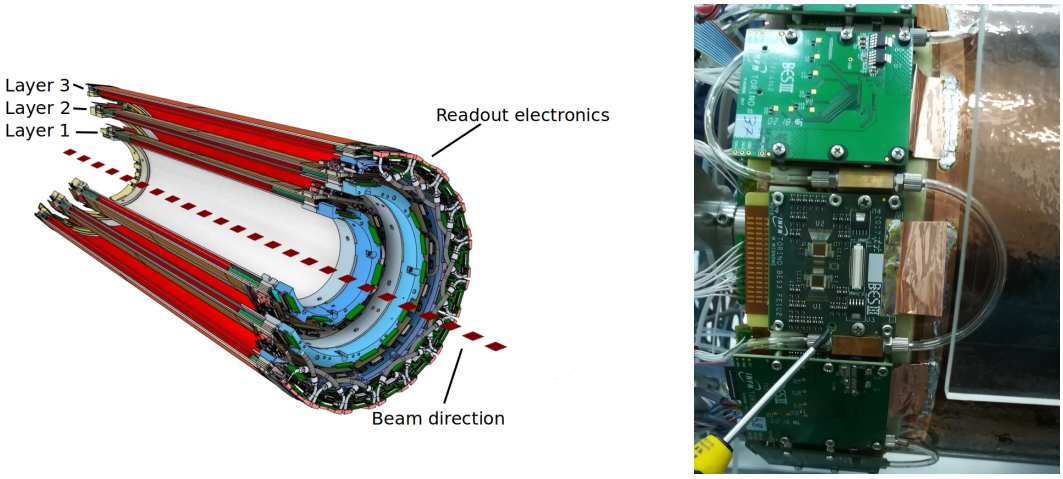

Figure 2: On the left: a cut-off of the CGEM detector technical sketch. The readout electronics is located on both sides of the detector. On the right: front-end boards mounted on the detector. One board is removed to show the TIGER ASICs. A copper foil connects the front-end boards ground plane with the detector ground plane.

Since BESIII is expected to be in operation for the next ten years, an upgrade is needed. An innovative solution to replace the aging inner MDC is to use a CGEM Inner Tracker (CGEM-IT). It was proposed by the Italian Collaboration in BESIII and boosted by a European-Chinese network, funded by the European Commission. Indeed, GEM technology allows larger rate capability and reduced aging effects on the long period, therefore a longer lifespan.

The CGEM-IT is made of three coaxial layers of triple GEM (figure 2 and table 1). Each cylindrical detector layer is independently assembled, it has an autonomous gas enclosure and can be operated stand-alone. The front-end electronics, the electrodes connections and the gas inlet and outlet are

Layer	Inner diameter (mm)	Outer diameter (mm)	Active area length (mm)
1	153.8	188.4	532
2	242.8	243.4	690
3	323.8	358.5	847

Table 1: Dimensions of the CGEM-IT layers. The active area length is equivalent to the length of the Φ strips.

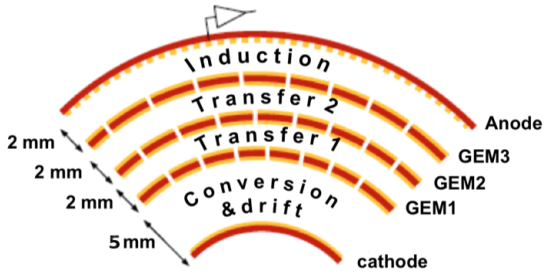

Figure 3: Single layer triple-GEM layout. Each detector layer is composed by cathode, anode and 3 GEM multiplication foils.

GEM voltages		Fields	
		Induction	5 kV cm^{-1}
G3	275 V		
		Transfer 2	3 kV cm^{-1}
G2	280 V		
		Transfer 1	3 kV cm^{-1}
G1	280 V		
		Drift	1.5 kV cm^{-1}

Table 2: Voltage across the GEM foils and transfer fields. The total GEM voltage of 835 V corresponds to a gain around 13500.

located on both sides of the cylinders. A GEM electrode is composed of a polyimide foil (50 µm) coated on both sides with a thin copper layer (5 µm), pierced with a high density of holes (50 µm diameter) with a pitch around 140 µm. Applying some hundreds of volts (200 V–300 V) between the copper foils, a 50-100 kV/cm electric field is generated and the electrons accelerated into the holes are thus multiplied [5].

In a triple-GEM (figure 3), the ionisation electrons, produced in the gap between the cathode and the first GEM foil (conversion and drift gap) by the charged particles crossing the detector, are guided by electric fields (transfer fields) through the three GEM foils where they start electron avalanche. Once they cross the last GEM foil they drift to the anode in the so-called induction gap, giving rise to an induced current signal on the anode plane. Several stages of amplification guarantee a high gain of the detector with a low discharge probability.

The CGEM-IT uses a mixture of argon and isobutane (90%-10%). The GEM voltages and fields settings are shown in table 2. To set electric fields in the gaps, seven different electrodes need to be biased: the two copper planes of each GEM and the cathode (section 6). The readout circuit is made by 3 µm copper cladding over 50 µm polyimide. Two arrays of strips are used in order to obtain a 2D readout: 570 µm wide Φ strips, parallel to the detector axis, and 130 µm wide V strips, having a stereo angle with respect to the Φ strips (see figure 4). The stereo angle is maximized according to each layer active area: 46.7° for the innermost layer (layer 1), −31.0° for the central layer (layer 2) and 32.9° for the outer one (layer 3). The pitch, 650 µm, is the same for both arrays and all the layers.

The full system consists of about 10,000 electronics channels. Being a tracker, the first goal of the CGEM-IT is a precise position determination, with an expected resolution of 130 µm in $r\phi$ plane

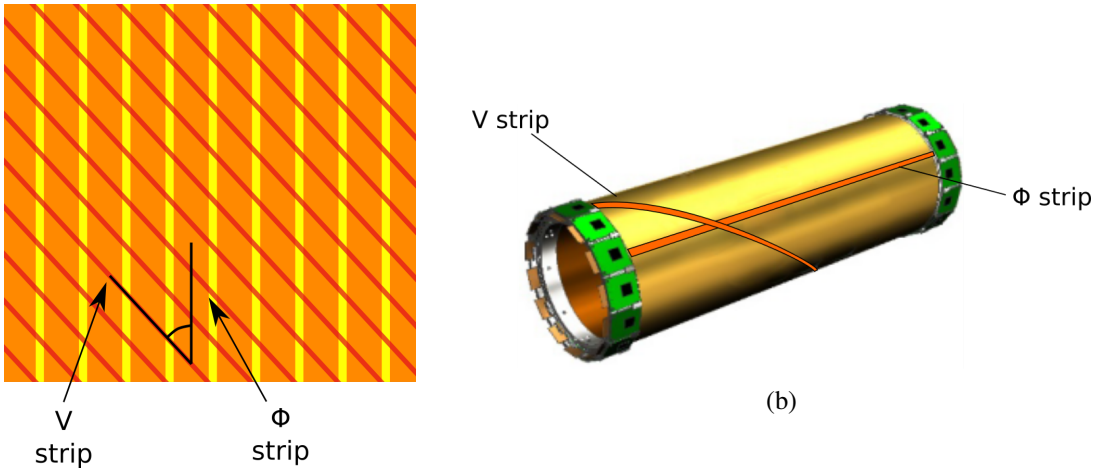

Figure 4: Strip layout. (a): the anode structure for layer 1, with the Φ strips in orange, the V strips in red and the 46.7° angle between them in black; (b): a sketch of the anode strips orientation on the cylindrical structure.

$r\phi$ resolution	130 µm
z resolution	<1 mm
σ_{p_t}/p_t	0.5 % at 1 GeV/c
Material budget	1.5 % X_0
Maximum rate	10^7 Hz/cm^2

Table 3: Design goals of the CGEM-IT detector.

and 300 µm on the z coordinate, along the beam direction [6]. The main design goals are listed in table 3. In particular, the CGEM-IT is expected to improve the z determination and the secondary vertex position reconstruction with respect to the MDC [7]. The position reconstruction will take advantage from the combination of two different algorithms:

- Charge Centroid extracts the average position weighting the signal amplitude of the firing strips.
- µTPC (micro Time-Projection Chamber) uses the drift gap like a time-projection chamber. The positions of the primary ionizations in the drift gap are reconstructed by knowing the drift velocity and the arrival time of the signal at the anode. Then the points are fitted in order to extrapolate the position of the tracked particle in the gap center [8, 9].

These algorithms and the BESIII environment pose specific requirements on the readout features in terms of charge measurement, time resolution and sustainable rate, making the design of a dedicated readout chain necessary. This paper describes the readout chain of CGEM-IT. The system overview is shown, pointing out the main requirements for the front-end and back-end electronics, including the power distribution systems. It is reported how the system has been designed and tested. Finally,

a dedicated software interface has been developed in Python with control, monitoring and logging functionalities; its main features are also shown.

2 System overview

The overall readout chain needs to sustain a peak rate of 14 kHz/strip of signal hits for the strips of the innermost layer [10]. In order to ensure that the system will have enough bandwidth and rate capability headroom to accommodate signal and noise, the rate has been multiplied by a factor of safety equal to four, hence a system with a capability of 60 kHz/channel is needed.
Other specific requests were posed by the reconstruction methods: the Charge Centroid requires an analog readout, while the μTPC, in order to achieve the needed performance, requires an electronics contribution to the time resolution better than 5 ns.
The designed readout chain is shown in figure 5.
The TIGER chips (section 3) are assembled in pairs on Front-End Boards (FEB) and installed on the detector. Data and ASIC Low Voltage (LV) are fed through Data Low Voltage Patch Cards (DLVPC) by the GEM Read Out Cards (GEMROC). The connection from GEMROC to DLVPC is made through long haul cables (8 m and 10 m long for data and LV, respectively), while flexible short haul cables (1.2 m long) are used inside the spectrometer between DLVPCs and FEBs.
The GEMROC boards receive signals from the BESIII timing and trigger interface, communicate with the BESIII slow control via Ethernet interface and via optical fibers with the GEM-Data Concentrator (GEM-DC) cards, which build the events and communicate with the VME-based BESIII DAQ. The GEMROC boards also manage the front-end boards power supply and configuration as well as the TIGER output data collection (section 4).
The requirements met for the CGEM-IT project make the electronics also suitable for the readout of other innovative micro-pattern gaseous detectors with similar signal characteristics. For such reason, the whole readout chain was designed keeping in mind strong adaptability and modularity.

3 Front-end electronics: TIGER ASIC

TIGER (Torino Integrated GEM Electronics for Readout) is the ASIC designed for the readout of the CGEM-IT strips [11]. Each mixed-signal chip can handle the complete readout of the data incoming from 64 channels, providing time and charge measurement in order to satisfy all the design requirements (table 3) .
On each channel (figure 6), the signal is amplified and inverted by a three stage cascoded common source Charge Sensitive Amplifier [12]. The signal is then duplicated to feed two different shaping branches, one optimized for time measurements (60 ns peaking time) and the other optimized for charge measurements (170 ns peaking time). The fast rising time on the time-optimized branch provides low jitter time measures (T branch), while the flatter peak on the charge-optimized branch allows to sample the peak voltage with optimized Equivalent Noise Charge (ENC) for accurate charge measurements (E branch).
On both branches, a fine time measurement can be performed using a time to amplitude converter combined with a Wilkinson ADC, pushing the time resolution below the clock period (6 ns for BESIII). The jitter on the T branch dominates the final resolution (see table 4), while the resolution

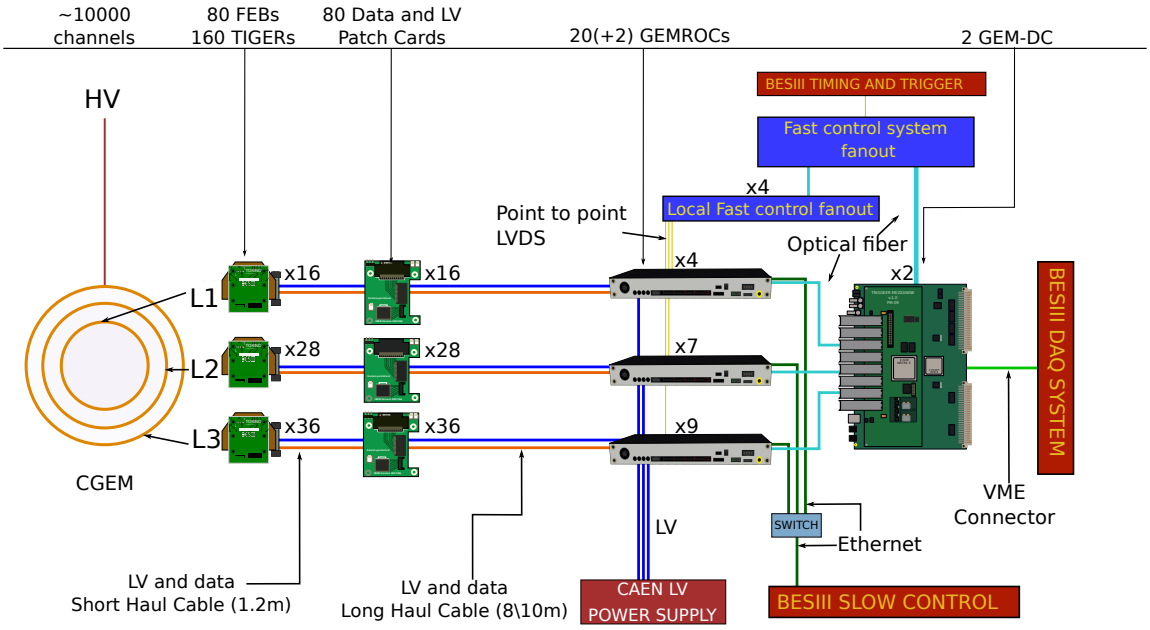

Figure 5: Scheme of the full readout chain. The ~10000 CGEM-IT detector strips are read by 160 custom ASICs (TIGERs) mounted on 80 front-end boards. The front-end boards are managed, four by four, by the GEM Readout Cards, FPGA based modules which control the ASIC low voltage, configure the ASIC and select the data. The selected data are then collected by two GEM-Data Concentrator cards and sent to the main BESIII DAQ. The fast control system fanout receives the timing signals from the BESIII main system and delivers them to its subsystems.

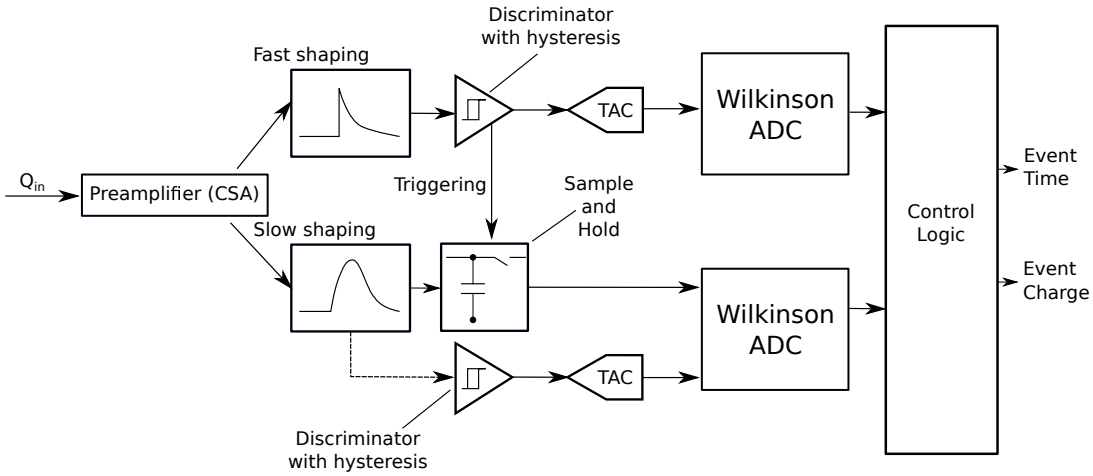

Figure 6: Overview of TIGER channel architecture. After the preamplification, the signal is split in two branches optimized for time and charge measurements. Each branch is equipped with TACs and Wilkinson ADCs for time measurement. On the slow shaping branch (the E branch), the Wilkinson ADC can be used to measure the charge stored by the Sample-and-Hold.

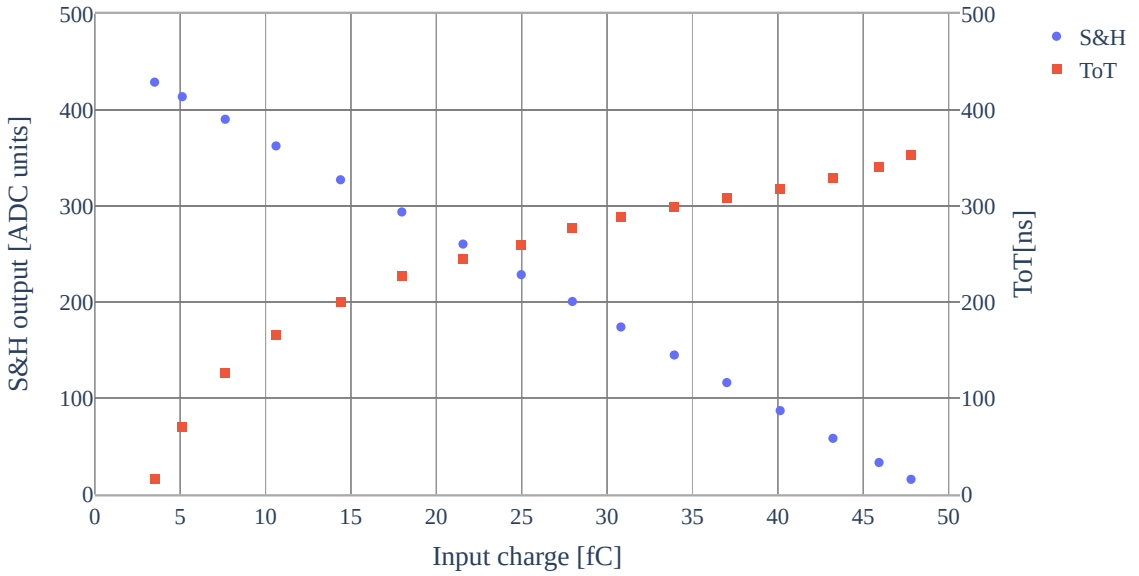

Figure 7: Sample-and-Hold (S&H) and Time-over-Threshold (ToT) calibration curves for one TIGER channel.

of the TDC is better than 50 ps.

TIGER does not need an external trigger to operate, since it has one discriminator on both branches. The great flexibility of the digital part of the ASIC allows to use many combinations of the discriminator triggers to validate the signals.

The thresholds on the branches discriminators can be set independently for each branch and each channel with 6 bits DACs, while the control logic enables to set various hit validation triggers using both discriminators.

The charge can be measured in two different modes: Time-over-Threshold and Sample-and-Hold mode. With the Time-over-Threshold mode, TDCs of both branches on each channel are used to measure the rising and the falling edges of the signal, thus obtaining the signal amplitude. The time information can be acquired on both shapers' output using different configurations.

In Sample-and-Hold mode, the signal on the E Branch is stored on a capacitor at a settable time after the threshold crossing, in order to sample its peak value. Then, the stored signal is digitized using the Wilkinson ADC shared with the TDC, providing a linear relationship between the digital output and the input signal amplitude. The comparison between Sample-and-Hold and Time-over-Threshold typical calibration curves is shown in figure 7. The Sample-and-Hold mode is the one chosen for the CGEM-IT readout since it is more robust to differences of the detector signals duration. Its calibration is linear and less threshold-dependent than the Time-over-Threshold one.

The ASIC outputs three kinds of data words: hit words, containing the hit information in 54 bits; counter words, used for debugging to count the hits on a channel; and frame words, sent every 2^{15} clock cycles, for time reference.

Input dynamic range	2-50 fC
Gain (E branch)	11.8 mV fC^{-1}
Noise (E branch)	< 1800 e^- ENC (0.29 fC)
Jitter (T branch)	< 4 ns
Sample-and-Hold residual non linearity	< 1% in the whole dynamic range

Table 4: TIGER key performance measured on silicon with C_{in} =100 pF and Q_{in} =10 fC.

The ASIC digital back-end and the full-digital interface are inherited from the TOFPETv2 ASIC [13]. Four TX LVDS links can transmit the data in 8b/10b encoding, up to 200 MHz in both Single Data Rate and Double Data Rate, while ASIC internal registers are programmed via a 10 MHz SPI-like configuration link. In TIGER, triple redundancy of the digital registers has been added to ensure Single Event Upset protection to operate in a high radiation environment.
The ASIC performance is summarized in table 4 [14].

The ASICs are mounted in pairs on front-end boards. Such boards are composed of two different PCBs, mounting a Hirose FX10A144P connector for the interface with the detector strips and the circuitry necessary for the power supply, the biasing, the channel protection and the ESD protection. A cooling system has been designed to stabilize the FEB temperature, to ensure an operation of the ASIC at an almost constant temperature and to limit the heat dissipation towards the outer MDC. Each FEB mounts a custom designed copper heatsink. The delivery and the exhaust are made through polyurethane radiation-resistant tubes. The heatsinks are grouped in order to limit the pressure drop per layer. In BESIII, the CGEM-IT cooling system will be connected to that of the EMC, using a booster pump and a patch panel with three lines in and three lines out per detector side. The cooling system keeps the temperature of the FEBs between 25 °C and 30 °C by circulating chilled water at 20 °C, 2.5 l/min and 2 bar. The thermal load is about 3.2 W per FEB (half for the ASICs and half for the voltage regulators), for a total of 256 W for the whole system.

4 Back-end electronics

GEM Read Out Cards (GEMROC) are the modules designed to configure and read TIGERs. Each GEMROC handles four FEBs, for a total of eight TIGERs. The core of each GEMROC is a development kit based on an FPGA of the Intel/ALTERA ARRIA V GX family [15], which is connected to an interface card designed for the BESIII experiment.

The GEMROC modules distribute digital and analog supply voltages to the FEBs, monitoring their supply currents and operating temperatures, via thermistors installed on the FEB, to ensure safe operation of the on-detector electronics. The whole system can be readout using 20 modules, but, to assure a symmetric distribution scheme of the two sides of each layer, 22 will be used.
The GEMROC modules receive, through a suitable distribution system, the timing signals forming the BESIII Fast Control System:

- *Clock*: BESIII distributes a 41.65 MHz clock, corresponding to the radio-frequency of the BEPCII storage ring divided by 12. The GEMROC derives all the time references from this signal. The GEMROC FPGA uses internal PLLs to derive signals toggling at a frequency of 166.6 MHz, four times the BESIII clock rate, to drive the TIGER clock inputs.

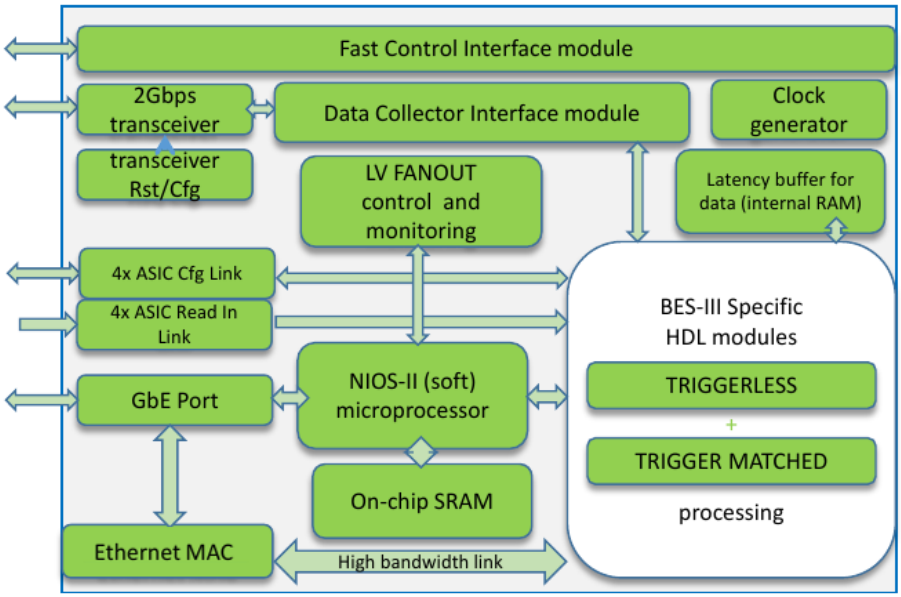

Figure 8: FPGA firmware blocks design. The I/O links are shown together with the main functional blocks. The system integrates both FPGA HDL blocks, in charge of the data processing and I/O managing, and a NIOS-II processor, used to manage the low voltage monitoring and control, the system diagnostic and the GEMROC configuration.

- *L1 trigger*: the BESIII level 1 (L1) trigger is used by BESIII DAQ and by the CGEM-IT readout system to mark event data to be saved. It has a rejection rate around $1 : 10^4$, a latency, with respect to the event, fixed at 8.6 µs, an acceptance window of 1.6 µs, an average frequency of 4 kHz and a dead time of 3 µs. The trigger signal lasts 8 clock cycles [16].
- *Check*: every 256 L1 triggers, a *check* signal is sent to verify the subsystems synchronization. This line can also be used, when operating in standalone mode, by the GEMROC modules for debugging purpose (*e.g.* to synchronize the test pulse generation).
- *Full*: this signal is used by all BESIII subsystems to notify that the buffers in which the event data are held, pending transmission to the DAQ, are filling up. When the BESIII Fast Control System receives the FULL signal from any of the sub-detectors, it stops sending further L1 triggers.

The FPGAs are programmed to control the system data acquisition; the firmware blocks are shown in figure 8. The firmware is written partly in Verilog and in VHDL languages. The GEMROC modules can handle the data received from the FEBs in two different ways. In the first one, called trigger-less (TL), used in standalone configuration for debugging purposes, the data received from the enabled TIGERs are merged and transmitted over the Ethernet output port using the UDP protocol. A UDP packet, limited to the standard size of 1500 B, is transmitted either when it contains all data collected in eight TIGER time frames (2^{15} TIGER clock periods) or when the number of TIGER collected data words reaches 180, with the remaining part of the TIGER data being transmitted in following UDP data packets.

Differently, in trigger-matched (TM) mode, a finite state machine selects the hits to be sent over in the following way: the data incoming from each couple of TIGERs are stored in a *latency buffer* circular memory, which is organized in pages of 32 locations each. This memory is intended to buffer the incoming TIGER data, pending the L1 selection trigger. A latency buffer page, also defined bucket, contains all the data recorded by the two TIGERs of a FEB in a time interval corresponding to 2^8 TIGER clock cycles (1.53 µs). The bucket memory is circular, so data are overwritten every address rollover (24.6 µs). The paged organization of the latency buffer is meant to speed up the search, started when the L1 trigger signal is received.
When the BESIII trigger arrives, the FPGA logs the trigger time of arrival timestamp, waits for a programmable delay to account for the stochastic transmission latency of the data over the TIGER output serial links, and then reads the buckets determined by the L1 trigger time of arrival timestamp to search the TIGER data with coarse event timestamps falling inside the BESIII trigger window. The hits from all the FEBs connected to a GEMROC and enabled to data taking are merged to prepare a trigger-matched data packet to which a header and a trailer are added. The L1 trigger to which the data were matched can be properly identified through the header and trailer. The latter contains also diagnostic information about the GEMROC status.
The trigger-matched data packet is then sent over the fiber optic link to the GEM-DC modules and also sent as a UDP packet over the Ethernet port.
This last feature is exploited during standalone operation of the CGEM-IT setup and enables trigger-matched data to be also collected by an alternative Ethernet-based data acquisition system.
The GEM-DC are VME 6U cards used to collect the trigger-matched data packets transmitted, via optical links, by the GEMROC modules and to assemble them into sub-detector events identified by the common trigger number. A VME interrupt is then generated by the GEM-DC to prompt the VME crate CPU to read the trigger-matched events stored in the GEM-DC buffers. The GEM-DC boards inherit the hardware design and most of the firmware from the Read-Out Driver (ROD) modules used by the KLOE-2 inner tracker [17].
Each FEB is connected to a GEMROC via short-haul and long-haul shielded multiple twisted-pair (MTP) cables interconnected through the DLVPC boards. The MTP cables feature relatively low losses but, due to the length of the data path and the unavoidable discontinuities, the fast signals exchanged between GEMROC and FEB, and the TIGER clock in particular, have been found susceptible to EMI and ground noise. This causes transmission errors that are detected thanks to the error detecting features of the 8b/10b encoding of the TIGER serial outputs.
To improve the signal integrity issues, a set of patch cards have been installed on the interface card of the GEMROC modules; these cards feature an LVDS driver with pre-emphasis, which boosts of about 20 % the amplitude of the TIGER clock signal received by the FEBs, resulting in a signal level well matching the input specifications of the clock receivers on the FEBs.
To improve the quality of the fast control signals (FCS) and overcome the signal integrity issues, an upgrade of the fast control signal distribution system has been carried out. The upgraded FCS distribution system consists of a System FCS Fanout module driving four Local FCS Fanout modules, located near the BESIII DAQ system and near the CGEM-IT GEMROC modules respectively. The GEMROC modules are grouped at four locations around the BESIII detector. Therefore, four Local FCS Fanout modules are being assembled.
The System FCS Fanout is interfaced directly to the BESIII FCS System and it is connected to the

Local FCS Fanout by bidirectional optical links operating at frequency from DC to 50 MHz. The Local FCS Fanout modules use transceiver daughter cards to drive the received electrical signals onto a multi-drop backplane with single-ended signaling. Up to six Flat-Cable Port (FC-Port) daughter cards are also installed on the Local FCS Fanout backplane. The FC-Port cards feature a 10-pin connector for the flat cable segments onto which the output LVDS signals are delivered to the destination GEMROC module.
The System FCS Fanout is programmable and may simulate the BESIII timing signals to test the CGEM-IT in standalone mode.

5 Low Voltage distribution

The power distribution design is based on the following FEB bias requirements: 1.08 A at 1.4 V for the ASIC analog part, 0.32 A at 2.5 V for the ASIC digital circuitry. A further requirement for the LV power system is to provide the GEMROC modules with a bias voltage of 15 V with an average current consumption of about 1.1 A.
The power supply system uses the following commercial modules provided by CAEN S.p.A.:

- One SY4527LC mainframe [18] (600 W max) and three A2517 boards [19] (24 channels, max 5 A/channel and 50 W/channel) to supply the FEBs;
- One SY5527 BASIC mainframe [20] (600 W max) and four A2519 boards [21] (32 channels, max 5 A/channel and 50 W/channel) to supply the GEMROC modules.

One pair (analog and digital supplies) of output channels of the CAEN A2517 is parallel-connected to the FEB power input of two GEMROC boards, which, in turn, deliver and monitor the analog and digital power supplies to eight FEBs.
Such modularity of eight was chosen because it well matches to the dimensions and complexity of the GEMROC modules and allows to keep a separate ground reference for each detector layer when 22 GEMROC modules are used.
All power supply cables are shielded and equipped with connectors to refer shields to the ground net. The length and the current capacity of the cables used for the LV power distribution are hereafter detailed:

- from the mainframe rack to the GEMROC:
  - GEMROC supply cable: 17 m, carrying (at most) 2 A;
  - FEB supply: 17 m, carrying (at most) 9 A (analog+digital);
- from the GEMROCs to the DLVPCs: 10 m, carrying (at most) 1.1 A;
- from the DLVPCs to the FEBs: 1.2 m, carrying (at most) 1.1 A.

Throughout the whole LV distribution system, the IR drop is a concern but the toughest constraints are for the cables which are connected between the CAEN A2517 cards and the GEMROC modules; for these cables the four wires section is 4 mm^2.
The power dissipation, considering the optimization of the TIGERs operating conditions, is expected

to be 330 W for the total number of FEBs and 484 W for the total of 22 GEMROC modules. It will be increased by the amount dissipated by the FCS Fanout system, which is estimated in 33 W for the FCS System Fanout and 22 W for the FCS Local Fanout.
To leave headroom to the power supply system, an A4532 Power Booster Unit will be installed in the SY5527 CAEN mainframe to add 600 W to its output power.
The LV power distribution system is equipped with hardware and firmware features to allow remote control at the level of the CAEN power supply mainframes and at the level of the GEMROC.
The CAEN boards control and monitor their individual output channels which provide analog and digital power to the groups of eight FEBs, while the GEMROCs distribute, control and monitor the power to the individual FEB. The LV power distribution system is managed, in standalone operation, by custom software at the FEB level and by the CAEN GECO system (see section 8) at the power supply mainframe level. Once installed the CGEM-IT inside the BESIII spectrometer, the whole system will be managed by the Detector Control System (DCS) [2].

6 High Voltage distribution

The description of the High Voltage chain is included to complete the picture of the power distribution systems and their interconnection. For each triple-GEM, seven different electrodes need to be biased (the two copper planes of each GEM and the cathode). One side of each GEM foil is segmented in macro-sectors, the other in micro-sectors. Each macro-sector is matched by 10 micro-sectors. The cathode electrode is not segmented. The subdivision of the electrodes allows to reduce the energy involved in the case of a GEM discharge and to disconnect a part of the detector in the event of a short-circuit between GEM foils.The number of sectors depends on the layer size: for each GEM, there are 4 macro-sectors for layer 1, 8 for layer 2 and 12 for layer 3. The layer 1 electrodes are etched on a single sheet, while those of layer 2 and layer 3 on two sheets, glued together.
The HV distribution for layer 1 is shown in figure 9. The electrodes are powered from both sides of the cylinder ("gas in" and "gas out"), in order to optimize the space.
CAEN A1515CG boards [22] will be used as main generators, hosted in a SY4527LC mainframe [18]. CAEN A1515CG are boards designed to supply triple GEM detector, providing seven floating outputs on the corresponding detector electrodes. The HV reference ground is connected through a 10 kΩ resistor to the ground plane of each layer. The boards are interfaced through a Radiall-REDEL converter to a custom passive distribution patch-panel that splits the seven inputs into all the levels necessary to power the detector. Each output connector supplies two macro-sectors and the related micro-sectors. A full panel supplies up to 18 macro-sectors and the related micro-sectors. The panels allow to disconnect single sectors for diagnostic purpose or to isolate a shorted micro-sector.
The supplies, the Radiall-REDEL converter and the distribution panel will be hosted on the platform located on top of the spectrometer. For the off-dectector routing, braid shield and halogen free cables, rated up to 4.5 kV, will bring the power from the patch panels to the HV connectors cards inside the spectrometer. The appropriate shielding of these 18 m long cables is essential to lower the HV induced pick-up noise of the system. The 2 m long cable for on-detector interconnections has to be light, multi-core and flexible to allow routing in tight spaces. Custom small-section and

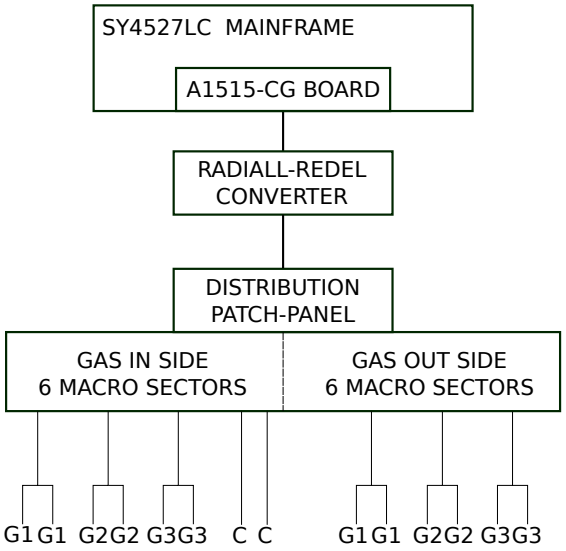

Figure 9: Block diagram of the layer 1 HV distribution system. Each multi-core cable departing from the distribution patch-panel comprises two macro-sectors cables, the 20 corresponding micro-sector cables and six reference ground cables. The power line splits in the two macro-sector cables for the last meter before the detector.

low-weight cables have been assembled using extruded FEP insulated cables. For the same reasons of size and weight, custom connectors for off-detector/on-detector connections were designed. The connectors are composed of two boards which are inserted one into the other. The electrical insulation is ensured by a protective coating and by 3D printed plastic enclosures.
The connectors towards the CGEM-IT are similar to those of interconnections. Since the tight space does not allow to install any enclosure, the electrical insulation is ensured by the board clearance and by the insulating coating. They mount protection resistors (1 MΩ for macro-sectors and 10 MΩ for micro-sectors). The coupling between the protection resistors and the macro/micro-sectors capacitance provides RC filtering on the HV lines.
All power supplies are fully floating and each supply has its own return path. The whole detector is located in a Faraday cage. The detector module is connected to earth at only one point (star structure).

7 Occupancy and data rate

As seen in section 2, the maximum hit rate per channel for the CGEM-IT detector in the BESIII experiment is about 60 kHz, considering a factor of safety.
The system is well-sized to address the experiment rate. Great flexibility in the delay tuning and the thresholds settings allows to allocate the resources to maximize the performance taking into account the noise and background differences among the layers and the strips.

The TIGER ASIC was tested to assess its maximum sustainable hit rate: figure 10 shows that the TIGER can digitize at a hit rate per channel up to 300 kHz. Figure 11 displays that the ASIC can maintain its accuracy in charge measurements at hit rates per channels up to 70 kHz, even with

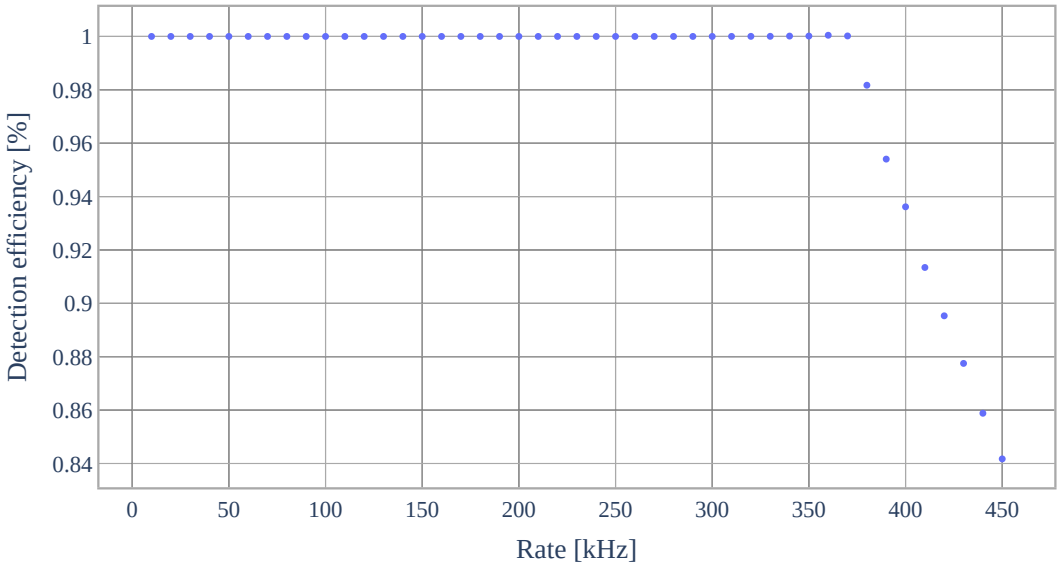

Figure 10: Digitization capability of a single TIGER channel. The measurement is done with an externally generated voltage square waves injected in the channel under test for 10.000 times at different rates and then the number of digitized hits is counted. The statistical errors are negligible.

large signals of 40 fC. For the CGEM-IT operation, where we can expect an average input charge of 8 fC–10 fC and a physics hit rate of 14 kHz/strip, the difference between the charge measured and the charge according to the calibration is within the relative uncertainty (3 %) of the Sample-and-Hold noise [14] and should not affect the charge-centroid resolution.

The two LVDS, 8b/10b encoded, serial data links driven by each TIGER at a rate of 332 Mb/s enable the transfer of hit data at a maximum lossless rate of 4.15 MHz, equivalent to 65 kHz per channel assuming a flat distribution of hits in time. The TIGER performance is thus more than adequate to cope with the BESIII expected data rate.

The GEMROC modules have enough resources to accommodate the input and the output data rates. A set of rate-leveling input FIFOs in the GEMROC FPGA receives and offers temporary storage for the data from each pair of TIGERs on the same FEB. Data are then accommodated into a set of circular page-organized memory buffers, one per FEB, on which they are stored for the L1 latency period (plus some programmable delay to account for transmission latency) until the decision to save or reject them (see section 4).

At the expected background rate, an average of 12 memory positions will be occupied in each 32-locations page of the circular buffer, leaving a headroom of 20 locations for physics signals and noise, which is sufficient in response to a typical BESIII interaction with an average of six tracks, an average cluster size of 3, on both the Φ and the V views on each layer.

Unused resources in the GEMROC FPGA are still available to increase the capacity of all storage devices described above if the need arises in the future.

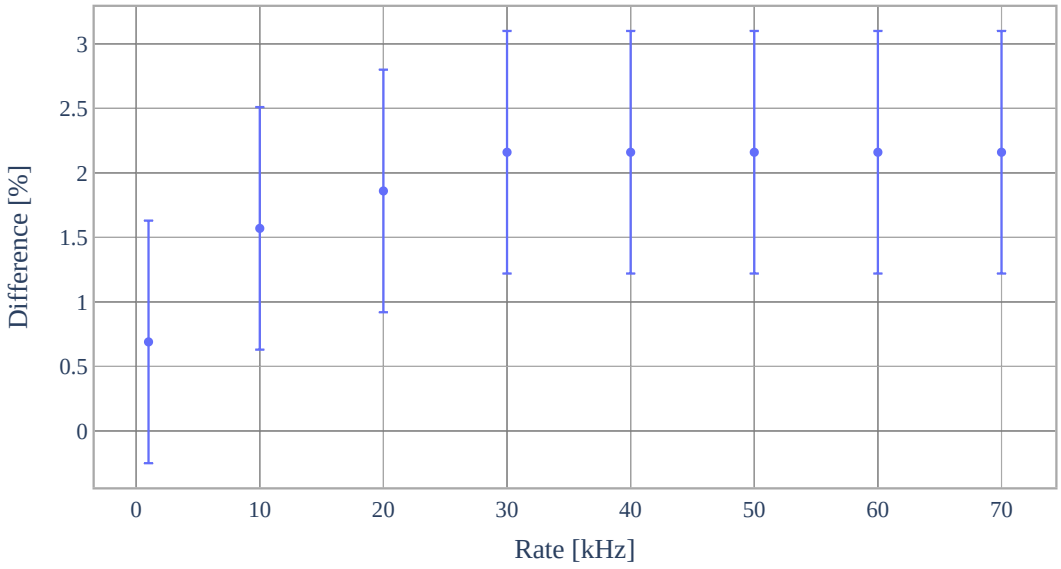

Figure 11: Difference between the charge measured and the charge according to the calibration, with respect to the rate. It was estimated for a fixed input charge of 40 fC, injecting a current pulse in one channel using a voltage generator and a capacitor. To generate an approximate single polarity current signal, the capacitance was rapidly charged (50 ns), and slowly discharged (14 µs). The error is the standard deviation of the measured charge.

The GEMROC output data rate is determined by the BESIII event rate, the L1 trigger rate, the L1 trigger window and the average trigger-matched event size.
According to the conservative estimate for the overall physics and background rate of 60 kHz per TIGER channel, an average hit rate of 3.9 MHz per TIGER is expected. Considering that the L1 trigger acceptance window width is 1.6 µs and that each hit information is encoded in an 8 byte word, the size of the TM data packet (including header and trailer) sent in reply to a L1 trigger would be around 410 byte. Taking into account that the average BESIII L1 trigger rate is 4 kHz, the data bandwidth for trigger-matched data amounts to slightly more than 1.6 MB/s per GEMROC and thus about 33 MB/s for the full detector.
These bandwidths are achievable by the GEMROC data processing modules and by the optical fiber and Ethernet communication ports.
The optical communication links between the GEMROCs and the GEM Data Concentrators operate at 2 Gbps. Since the serial data is 8b/10b encoded the resulting net bandwidth is 1.6 Gbps, or 200 MB/s, which is well above the TM data rate of 1.6 MB/s discussed above.
In the same scenario, the transmission of the average TM data packet over the optical link requires about 2.0 µs. The link transmission latency is negligible considering that the GEM-DC starts processing the input data as the TM packet headers are received, overlapping, therefore, data reception and data processing. Two GEM-DC modules are planned to read the 22 GEMROC, since

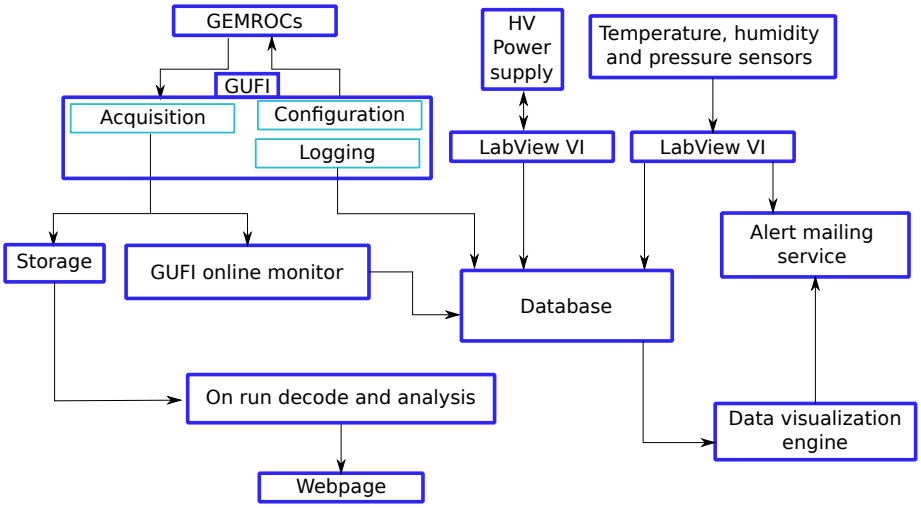

Figure 12: The acquisition and test control software infrastructure. Many parts of the software can be installed and run in different computers, since the communication takes place via UDP or TCP protocol.

each GEM-DC features 16 input optical transceiver ports.
The GEM-DC supports a wide range of VME protocols over the VME backplane, including 64-bit double-edge asynchronous (2eVME) and synchronous (2eSST) transfers, as well as serial transfer protocols for the 8-lane 3.125 Gbps VXS port. Standard block transfers at 40 MB/s, initiated by interrupts from the GEM-DC, are currently used to readout the GEM-DC via the standard VME-based BESIII DAQ.

8 Control software

In order to characterize, debug and test the system before the installation, a control software was developed. This software (called Graphical User Frontend Interface - GUFI), written in Python, handles electronics operations and acquisitions via the UDP protocol. The software has an intuitive graphical interface in order to be easy to use and to better control the system multiplicity.
Beside the standard operations, (e.g. powering on the front-end electronics, writing the configuration and starting the acquisition), the software has advanced features:

- Scan of the communication delays for the LVDS links between GEMROCs and TIGERs, in order to establish the most robust possible communication;
- Threshold-scans in order to verify the channel condition and the noise levels;
- Threshold optimization algorithm: the software is capable to scan the 2D thresholds space to obtain a certain rate of noise. The desired rate can be chosen for each part of the system (Φ or V strips for each layer), to optimize the homogeneity of the noise;

- Diagnostics and slow control operations.

The software has also monitoring and logging functionalities. The pieces of information are written in an Influx-DB database [23], which can be queried directly or visualized via the Grafana interface [24]. The GUFI online monitoring part creates a copy of each incoming packet and sends them to an analysis software. In this way, it is possible to prioritize the data storage and use the remaining resources for the online data analysis. Indeed, the software interconnects with the GRAAL analysis software suite [25], in order to perform a fast online analysis of key features to assess the status of the detector.
The GUFI system, together with the acquisition logging, the environment logging and the HV status read by LabView VIs, allowed to operate remotely the detectors assembled in China during the COVID-19 outbreak. The scheme of the full software system is shown in figure 12.
The software is very flexible and can be employed in future tests with developments of the detector, other detectors and other readout chains.
In order to test the CGEM-IT operation, a system made of two, out of three, fully equipped layers has been set up in a facility at the Institute of High Energy Physics in Beijing. The setup composed of layer 1 and layer 2 is fully equipped with gas, power and cooling systems, readout electronics, and the computing needed to operate it. A cosmic-ray trigger exploiting plastic scintillator detectors in coincidence was also set up to allow the system to record and fully reconstruct cosmic ray events. This setup has been taking data since December 2019, testing the readout chain reliability and stability, while providing data for the development and the calibration of the analysis software.

For instance, GUFI is used to measure the noise amplitude and noise spectrum. For the noise amplitude, a test pulse is sent to each TIGER channel, one by one, using the integrated test pulse generator. While sending the test pulse at a fixed rate, the threshold is swept over all the possible DAC values. Assuming that the noise amplitude is Gaussian, the rate curve can be fitted automatically to obtain an estimation of the standard deviation for the noise distribution.
With this procedure, the noise condition of the full test setup can be assessed (figure 13). The difference in noise levels of Φ strips for layer 1 and layer 2 can be explained taking into account the different mechanical structure [26]: layer 1 deploys a carbon fiber anode supporting structure, which increases the capacitive coupling of adjacent Φ strips. Note that, as expected, the noise level of the V strips shows a trend following the strip length (figure 14).
To measure the noise spectrum, without saturating the Ethernet bandwidth, small sections of the setup can be acquired in trigger-less mode and the data analyzed via Fast Fourier Transformation in the frequency domain.
Optimization of the shielding and grounding scheme took advantage of the information regarding the noise and the communication stability of the system installed in Beijing. The same tools will be used during the final installation inside the BESIII spectrometer in order to optimize the setup grounding.

Important metrics for the detector status come from the data analysis performed at single-hit level by the DAQ software itself. Figure 15 shows the charge of the hits versus the time with respect to the trigger, acquired during the cosmic ray data taking. With this kind of plot we can verify the detector signal, the good synchronization of the system and the absence of other structures in time beside the signal. Figure 16 shows the charge in the signal time region versus the strip position

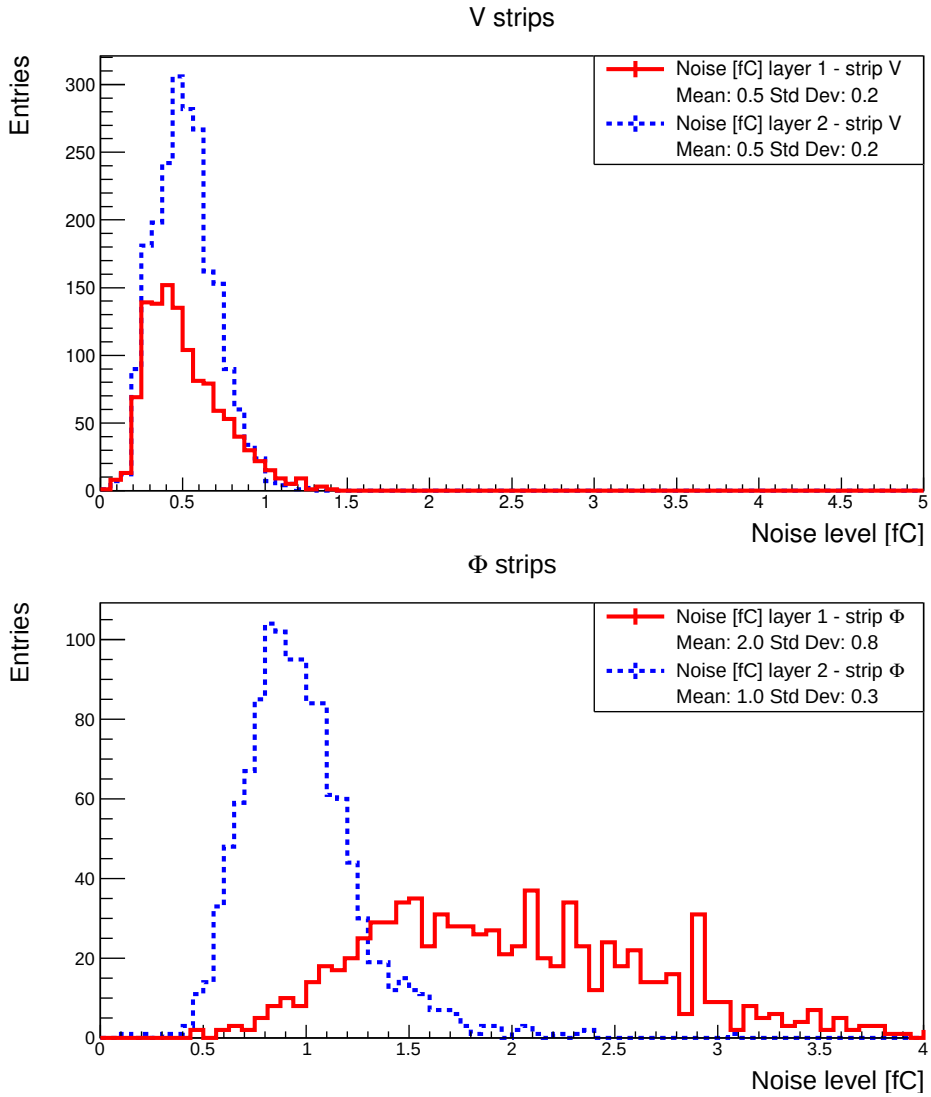

Figure 13: Noise level measured on layer 1 and layer 2, both for Φ and V strips, using the cosmic ray test setup in Beijing.

which permits to monitor the uniformity of the detector.

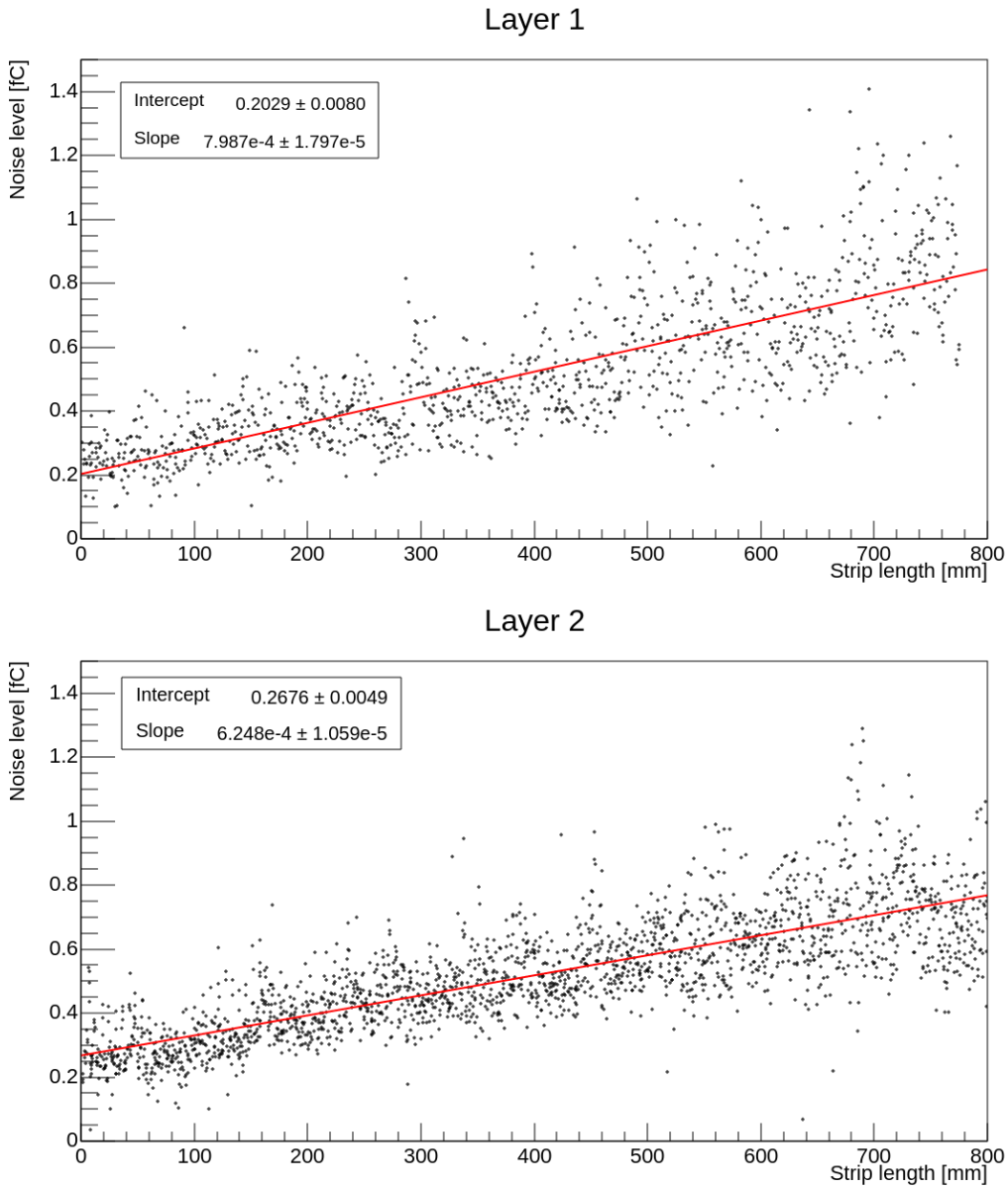

Figure 14: The trend of the noise vs the V strip length is due to the increasing capacitance of longer strips. The mechanical differences between the two layers determine the differences in slope and intercept. The parameters of the linear fit are reported in the legend.

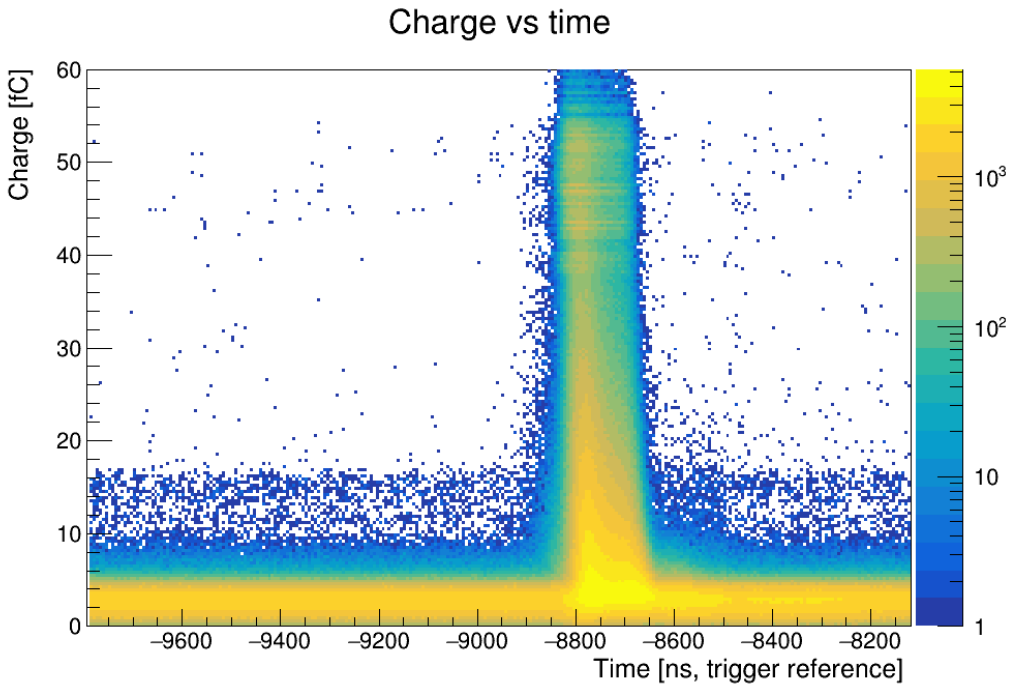

Figure 15: Hit charge versus hit arrival time with respect to the trigger arrival time on the layer 2, V strips. Data acquired during one week of cosmic rays acquisition. The broad central peak is the detector signal, while the low charge horizontal area is noise.

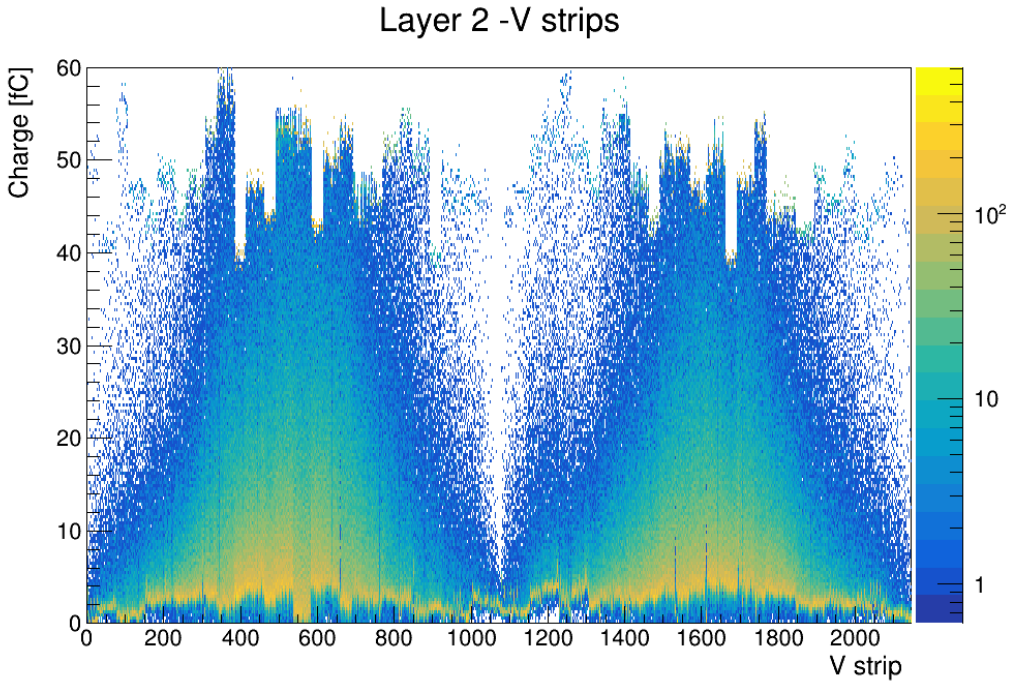

Figure 16: Charge on the layer 2 V strips in the signal time region. The charge is mostly distributed on the longest strips (400–700 and 1500–1800).

9 Conclusions

The CGEM-IT detector readout chain has been successfully developed. A dedicated on-detector and off-detector electronics has been designed according to the required performance. The TIGER ASIC reads directly the detector strips, providing the full digitized charge and time information. Its specification are tailored for the modern micropattern gas detectors. The GEMROC modules provide power, timing and control signals needed for TIGER operation and receive and process the output data of TIGER ASICs. Downstream the GEMROC modules, the VME-based GEM-DC receive via optical links the trigger-matched data packets, assembling them into full events which are then made available to the VME-based BESIII DAQ system.
A dedicated system was devised for delivering and monitoring Low Voltage and High Voltage power to the the readout electronics and to the detector. This system was designed to provide detailed control and monitoring of the operating voltages and currents.
All the components have already been tested and proved to achieve the required performance. The detector electronics is now in the last phases of its commissioning and optimization.
The whole readout system was designed focusing on great modularity and could be used for other innovative detectors.

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This paper is dedicated to the memory of our colleague Stefano Cerioni.

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