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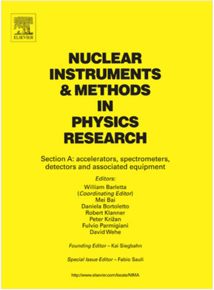

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Single Event Upset tests and failure rate estimation for a front-end ASIC adopted in high-flux-particle therapy applications

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Abstract

A 64 channels Application Specific Integrated Circuit, named TERA09, designed in a 0.35 μm technology for particle therapy applications, has been characterized for Single Event Upset probability. TERA09 is a current-to-frequency converter that offers a wide input range, extending from few nA to hundreds of μA, with linearity deviations in the order of a few percent. This device operates as front end readout electronics for parallel plate ionization chambers adopted in clinical applications. This chip is going to be located beside the monitor chamber, thus not directly exposed to the particle beam. For this reason, no radiation hardening techniques were adopted during the microelectronics design. The intent of the test reported in this paper is to predict the TERA09 upset rate probability in a real application scenario. Due to the fact that TERA09 has an extended digital area with registers and counters, it is interesting to estimate the effect of the secondary neutron field produced during the treatment. The radiation damage test took place at the SIRAD facility of the Italian National Institute for Nuclear Physics in Padova, Italy. The SIRAD facility allows to study the CMOS upset rate as a function of the energy deposited during irradiation. By irradiating the chip with ions of different Linear Energy Transfer, it is possible to calculate the single event effect cross section as a function of the deposited energy. It resulted that the minimum deposited energy in a CMOS silicon sensitive volume of 1 μm^3, responsible for a Single Event Upset probability higher than zero, is 690 keV. In the last part of the paper, we calculated the expected upset probability in a typical clinical environment, knowing the fluence of secondary, backward-emitted neutrons. Considering as an example a treatment room located at the CNAO particle therapy center in Pavia, the expected upset rate for TERA09 is $\sim 10^4$ events/year. Using a redundant and independent monitor chamber, the upset probability expected during one detector readout is lower than 10^{-24}, as explained in the document.

Keywords: Particle therapy, Monitor chamber, ASIC, CMOS radiation damage, SEU.

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1. Introduction

Since many decades parallel plate gas ionization chambers are the most used detectors in the cure of cancer with particles (protons and carbon ions). In this context, a single large area electrode is used for particle beam flux measurement whereas segmented electrodes allows the two-dimensional beam position measurements [1]. Ionization chambers require a multi-channel front-end electronics converting the charge with high accuracy operating with no dead-time. The collaboration between the University of Turin and the microelectronics group of the Italian National Institute for Nuclear Physics (INFN) designed and produced a family of Application Specific Integrated Circuits (ASIC), called TERA [2]. Tailored for clinical applications as front-end readout of gas detectors in particle therapy, the TERA chips are used in several clinical devices both for quality control in radiotherapy (e.g. the MatriXX detector [3] provided by IBA [4] and the monitor chambers developed by DE.TEC.TOR. Devices and technologies Torino [5]) and for beam monitoring in particle therapy facilities [6] [7]. The aging effects of the total ionizing dose were studied exposing the previous version of the TERA chip to an X-ray source. Results are reported in [8].

TERA09 is the last chip designed and characterized [9]. In this paper, the results of a Single Event Upset (SEU) test of TERA09 are reported and analyzed. Even though the ASIC is not going to be directly exposed to the particle beam, secondary neutron produced in the interaction with the nozzle, may induce temporary upsets which can occur in the digital circuitry.

A common procedure to characterize a CMOS device for SEU, is measuring the occurrence of the effect as a function of the energy deposited irradiating the chip with ion beams. Irradiation with ions of different Linear Energy Transfer (LET) is thus required for varying the deposited energy. The SIRAD (Silicon RAdiation Damage) facility [10], located at the 15 MV Tandem of the Legnaro National Laboratory (LNL) of the INFN, offers the possibility to select among different ion sources and to change the beam flux and the beam incident angle on the Device Under Test (DUT). During the test, the DUT is placed inside a vacuum chamber, thus minimizing scattering and beam slowing which would occur in air.

The TERA09 SEU test focused on the identification of bit-flips occurring in the ASIC counters and registers. From the bit-flip cross-section as a function of the deposited energy, the failure rate with a given neutron rate and energy spectrum can be predicted. An example of application to a clinical environment will be presented and discussed.

2. Basics of Single Event Effects in CMOS electronics

In CMOS technology the reliability of a system to Single Event Effects (SEE), i.e. perturbation induced by the energy deposited by single ionizing particles, is an aspect getting worse (or at least getting more challenging), with the design detail downscaling. In this field it is common to refer to Single Event Effects (SEE), distinguishing among heavy and soft damages. Examples of heavy or permanent damages are the Single Event Burnout, a destructive effect and the Single Event Latch-up (SEL), a short-circuit that can lead to burnout if not mitigated in time, by turning off the power supply. However this procedure

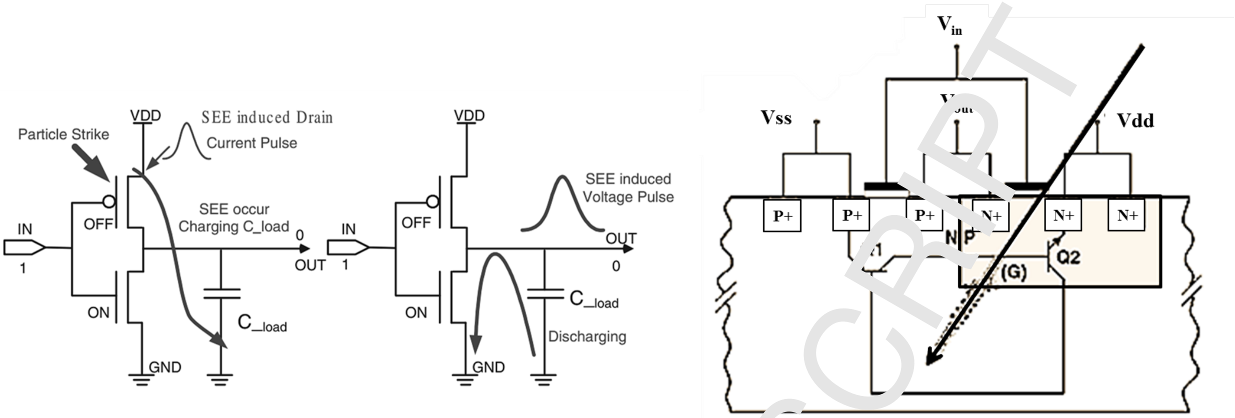

Figure 1: Left: schematic representation of an inverter bit-flip due to a SEU.
Right: The thyristor structure represented with the Q1 and Q2 bipolar transistors path. During a latch-up, both the BJTs are conducing resulting in a short circuit.

introduces some dead-time that could affect the data acquisition and should be considered as SEL consequence. In the soft event category, the Single Event Transient and the Single Event Upset (SEU) are the most common; the former results in a charge transient caused by a single proton or heavy ion passing through a sensitive node in the circuit whereas the latter results in a bit-flip, a logic state change due to energy deposition in a digital cell. Several studies proved that SEU and SEL effects are physically separated in terms of silicon region where they occur. SEUs are confined in the first micrometers thickness under the device surface whereas SELs occur deeper in the silicon bulk [11].

Single Event Latch-up occurs in deep volume of the the silicon bulk where, in a CMOS process, the combination of n-well, p-well and substrate forms a parasitic n-p-n-p structure called a thyristor (see Figure 1 right). During a latch-up both the BJTs are conducing, resulting in a short circuit, highlighted by the power supply compliance (activation of the current limitation circuitry). The permanent and destructive event is avoided turning off the power supply.

Single Event Upset in CMOS circuits can be important when exposed to high LET particles, due to the high released energy in the crossed medium. Hitting the silicon bulk, these ions create electron-hole pairs and their collection at the source/drain diffusion regions may result in a p-n junction current pulse, driving a voltage change in that node [12]. More in detail, in a CMOS structure a SEU happens if an ion strikes the channel region of a NMOS that is in its off state or if the ion strikes the drain region of an off PMOS. Considering the general notation of SEE, the event occurs whenever in a sensitive node the charge injected by the current pulse exceeds a given threshold value, represented as a critical charge Q_{crit}. In the left side of Figure 1 is shown an example of logic state switching occurring in a CMOS inverter. Considering the "1" logic state at the inverter input node, a charged particle striking the drain of the PMOS transistor induces a signal at its source; this signal charges the load capacitance. The discharge of this load capacitance results into an output voltage pulse (V_{out}), leading to a state-flip at the inverter cell output node. Considering the

TERA09 chip and its application, the study has been focused only on the SEU phenomena.

It is possible to model the SEU phenomenon with the following equation:

$$V_{out} \geq \frac{Q_{crit}}{C_{load}} = \frac{1}{C_{load}} \int_0^{t_{sw}} i_{ds} dt \tag{1}$$

where C_{load} is the load capacitance of the discharging path and t_{sw} is the time delay between the particle strike and the logic state change (voltage exceeding a certain threshold value). The drain-source current (i_{ds}) flows into the transistor of the SEU relevant node.

3. The Device Under Test

TERA09 is a 64 channels ASIC designed in a 0.35 μm process and taped-out in an Europractice multi-project wafer (the ASIC extended description and characterization is reported in [9]). This chip operates as the front-end readout electronics for ionization chambers and is designed for high-intensity ion-beams. The TERA09 has bipolar inputs, with a positive and a negative threshold control: once one threshold is crossed, a pulser block sends a charge quantum to the amplifier input. In this manner, the ASIC converts the analog information provided by the current integrated over the feedback capacitance of a differential folded cascode amplifier into the rate of charge quanta subtracted or added to this capacitance, according to the input signal polarity. This sequence is controlled by means of a finite state machine requiring four clock cycles and it avoids the amplifier saturation, thus obtaining a dead time free front-end. The high dynamic range of TERA09, allows a linear conversion in the range 3 nA - 750 μA, with a linearity deviation smaller than 4%.

The TERA09 block diagram representation is presented in Figure 2. The 64 identical independent input channels are fed into a current to frequency converter representing the front-end logic which is followed by a 32-bit counter and register; the data transfer between the former and the latter is activated with a digital load signal without adding a dead time, independently from the signal conversion operations. TERA09 integrates an adder tree, activated by the same load signal mentioned before and providing the sum of groups of 4, 16 and 64 channels. These values are stored in additional 34-, 36-, and 38-bit wide registers which can be addressed via seven digital Channel Select lines and read out on a 38-bit output bus through a multiplexer. This system is designed to allow reading directly the sum of the counters of 4, 16 or 64 channels if, in order to increase the dynamic range, the input current is split among these channels. A total of 2774 data bit storage, arranged in 85 data registers, covers a sizable area of the chip and may suffer data corruption, once the ASIC is exposed to external radiation.

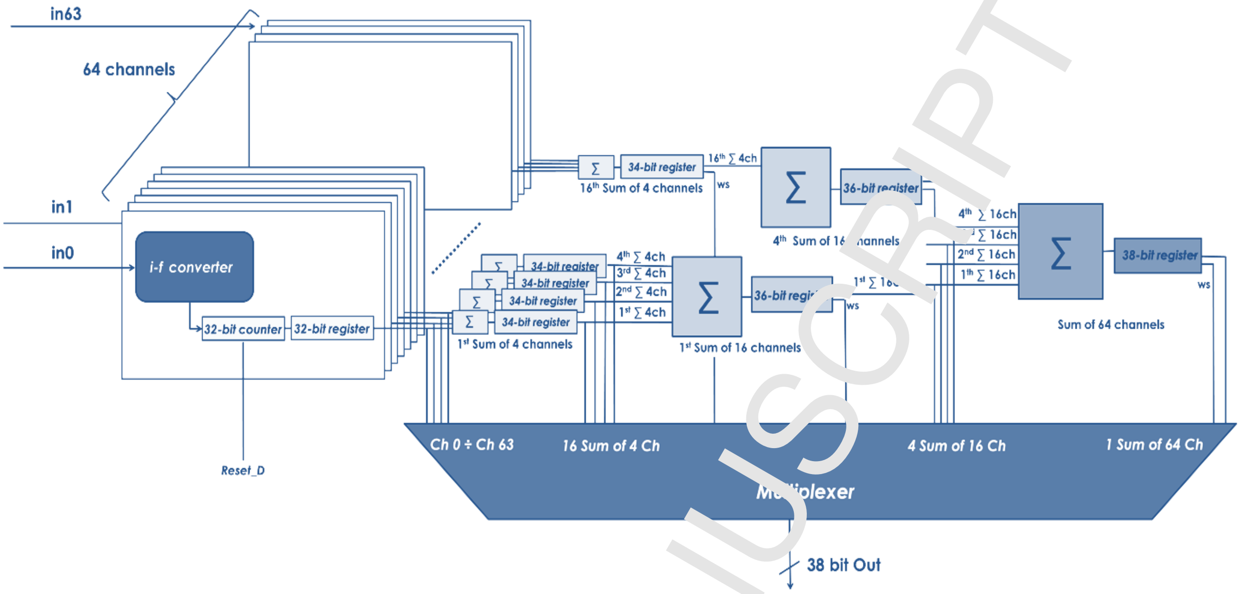

Figure 2: Block diagram of the TERA09 ASIC.

4. Test setup

The SEU phenomenon results as a bit flip originated by a high energy deposition of a single track in a small sensitive volume located into the digital circuitry. To study this effect in a controlled scenario, the particle flux rate must be carefully selected to be low enough to distinguish the effects caused by the impacts of single ions and high enough to observe a significant number of single effects in the measurement time. Typical ion fluence rate are in a range from 10^3 to 10^5 $ions \cdot cm^{-2} \cdot s^{-1}$ [10]. The experimental setup set for the SEU test consists of the TERA09, the device under test placed into a socket soldered on a PCB test board that interfaces the ASIC to the Data Acquisition System (DAQ), based on a Xilinx 7813R FPGA board configured through host PC with the LabVIEW for FPGA software toolkit. A voltage generator supplied the PCB 5V voltage, with a current limiter set to protect form burn-out due to a latch-up. The ASIC 250 MHz clock was provided externally with a LVDS signal source. The main goal of the DAQ software is checking how many times any bit of the 85 registers changes, due to upset events. In order to do that, the load signal used to transfer the data from the counter to the registers, was fixed as inactive, after a first trial acquisition run. A Keithley 2400 voltage generator was used to provide a steady current to the 64 inputs of the chip in order to let the counters increment rapidly after the power-up of the chip. This was necessary considering that upsets leading to a 0-1 bit and 1-0 transitions could occur with different probabilities and we wanted to measure the upset rate in a condition where zeros and ones are uniformly distributed in the register cells. Moreover, the registers content were also saved in a file for off-line analysis.

Along the SIRAD beam line, a vacuum chamber contains the metal plate for the DUT holding (Figure 3). The pressure in the vacuum chamber was set to $\sim 8 \cdot 10^{-6}$ mbar [10].

The holder is mechanically controlled by the user who can retract the DUT during the setup of the accelerator and then align it in front of the beam for the measurement. Moreover, the vacuum chamber is equipped with two sets of silicon diodes, one fixed and the other one movable (Figure 3). The fixed diodes are located in front of the final beam collimator and are used to monitor the beam fluence during the irradiation. Before starting the measurements, the DUT is kept in a retracted position and the beam is centered and focalized with the aid of a scintillator imaged by a CCD camera. Then, the fixed diodes are cross-calibrated with the movable silicon diodes which are temporary inserted in the position where the DUT will be placed during the tests. At the end of the calibration, the movable diodes were retracted.

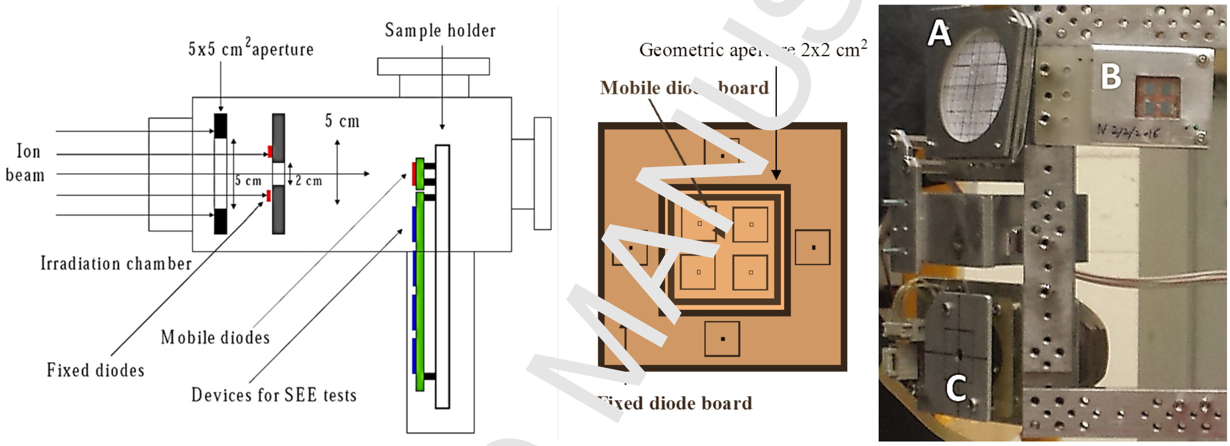

Figure 3: Schematic drawing of the irradiation chamber with the dosimetry system and the device under test holder (left). Diodes geometry and placement scheme (center). Right: vacuum chamber inner picture: A) scintillator; B) fixed diodes; C) movable diodes.

The TERA09 ASICs are packaged in a MQFP 160 pins ceramic structure. The chip is then carried by a plastic socket. In order to expose the 4.68 x 5.8 mm^2 silicon area of the chip, the ceramic cover of the package was removed and a hole was drilled in the socket.

All the interconnection cables were adapted or customized for the SEU test, in order to setup the data transfer through the vacuum chamber. The differential clock was provided via SMA cables. From a control room, outside the accelerator area, a remote desktop was used to set and control the DAQ and for the on-line monitoring of the raw data. With the adopted test procedure, the signal that loads the registers with the counters content was turned off after the initialization phase. At that point, any change in the registers is considered as originated by bit flips are due to SEUs. An iterative control every 100 ms checked the 2774 memory bits and a SEU counter was updated every bit-flip occurrence.

5. Results and data analysis

The SEU test performed with the TERA09 ASIC was devoted to the digital circuitry of registers. In this case, the focus is on the single bit flip due to a radiation-induced upset.

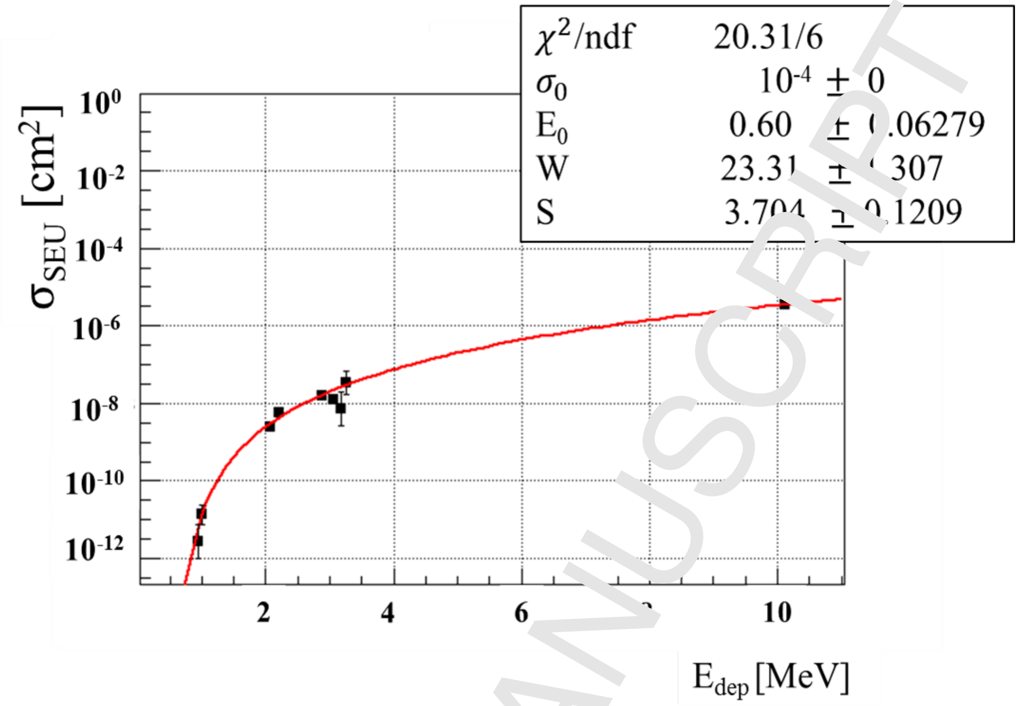

Figure 4: SEU cross-section as a function of the deposited energy.

The SEU cross section is defined as:

$$\sigma_{SEU} = \frac{N_{errors}}{\phi N_{bit}} \tag{2}$$

and corresponds to the probability per unit fluence and per bit cell of a bit-flip in the cell. Figure 4 shows the SEU cross section as a function of the deposited energy E_{dep}. The conversion from LET to E_{dep} was made according to [13].

As suggested by the approach described in [11], the Weibull function is used to fit the SEU cross section as a function of the deposited energy. The trend followed by this function describes those phenomena starting with a threshold activation mechanism and saturating at large values. The same method takes into account a $1 \times 1 \times 1 \mu\text{m}^3$ Sensitive Volume (SV) as the elementary reference volume where a SEU can occur. In SEU studies, E_0 is the the minimum energy that has to be deposited in the sensitive volume to trigger the upset event; the saturation level is the maximum SEU cross-section, due to the fact that each sensitive area is already affected by an upset. In a simple geometrical model, σ_0 should correspond to the effective sensitive area for SEU phenomena.

The Weibull function is:

$$\sigma_{SEU} = \sigma_0[1 - e^{-(E_{dep} - E_0/W)^s}] \tag{3}$$

where E_{DEP} is the energy deposited in the silicon; s and W are fit parameters.

Table 1: List of used ions and the corresponding energy, DUT-particle beam angle, deposited energy and cross section.

Ion	Energy [MeV/u]	Angle [°]	Edep [MeV]	σ_{SEU}
^{19}F	122	0	0.94	[illegible]
^{19}F	122	20	1.00	[illegible]
^{28}Si	157	0	2.08	[illegible]
^{28}Si	157	20	2.21	[illegible]
^{35}Cl	171	0	3.07	$1.88e^{-09}$
^{35}Cl	171	15	[illegible]	$7.10e^{-09}$
^{35}Cl	197	0	[illegible]	$1.53e^{-08}$
^{35}Cl	197	20	3.06	$1.21e^{-08}$
^{79}Br	241	0	10.12	$3.6e^{-06}$

The ions used for the TERA09 SEU test are reported in Table 1. The choice of the ion set was made considering that one needs data for both the threshold region and the saturation plateau. For ions with hight LET the measurement was affected by latch-up events in the silicon bulk. In these cases, the current limitation of the voltage supply avoided short-circuit destructive consequences. Using a bromine ion beam, corresponding to deposited energy of 10.12 MeV, the data acquisition was interrupted by frequent latch-up just after few seconds, thus allowing the acquisition of very short runs. No SEL events were observed with chlorine beam. As explained in the following section, given the relatively large deposited energy for the onset of SEL, no occurrence is expected in a clinical environment and no further investigations were attempted to determine the SEL cross-section. In addition, with ions lighter than fluorine, no SEU were observed. Changing the incident angle between beam and DTU allowed to slightly increase the deposited energy and to add a second energy-deposited point, for the same ion.

6. Expected SEU rate in a clinical room

The TERA09 ASIC follows the family of devices developed by our group that are equipping clinical monitor chambers worldwide. The previous versions of these chips, named TERA06 and TERA08 are routinely used in particle therapy centers like the National Center for Oncological Hadrontherapy (CNAO) [7] in Pavia, where our group has a consolidated role of research and technological collaboration since the center foundation. Since TERA09 has a more extended digital circuitry, compared to its predecessors, it is interesting to estimate the upset rate for TERA09 in a CNAO treatment room. The results of this study are hereafter reported. CNAO has a 25 m diameter synchrotron that accelerates protons and carbon ions in the energy range of 60 MeV - 250 MeV and 120 MeV/u - 400 MeV/u respectively. In the monitor chambers, the TERA ASICs are placed beside the gas volume and are not directly exposed to the proton beam flux; in this situation, the only source of upset events would be the secondary neutrons, backward emitted at the beam extraction point.

This hypothesis is supported by the data of Table 2 and the results reported in the same paper [14], where FLUKA Monte Carlo simulations show that the largest contribution that could be relevant for the radiation damage to the readout electronics are the secondary neutrons backward emitted by the interaction between the 400 MeV/u carbon ions and the target.

Table 2: Number of secondary neutrons and protons produced by carbon ion and proton beams on ICRU tissue (International Commission on Radiation Units and Measurements).

Target	**Primary particles**	**n/primary**	**p/primary**
$ICRU tissue$	$400 MeV/u\, carbon\, ions$	2.66	1.50
$ICRU tissue$	$120 MeV\, protons$	0.11	0.10

In this paper, a 3.4 10^{10} $n \cdot cm^{-2}$ annual flux of secondary neutrons at the nozzle, where the monitor chambers are located, was estimated using a 400 MeV/u carbon ion beam. Experimental data and simple theoretical arguments reported in [11] confirm that the SEU rate for neutrons and protons with an energy exceeding 20 MeV are expected to be equivalent. The probabilities per unit flux of an ionizing energy deposition larger or equal to E_{dep} in a sensitive volume were simulated in [11] for four different proton energies, yielding the results reported in Figure 5.

The choice of a sensitive volume of 1x1x1 μm^3 was justified by the authors as the one best matching the measured SEU cross section over 18 devices analyzed [11]. In a simplified model where an upset would always occur above an energy threshold, the 20 MeV proton data of Figure 5 could be interpreted as the SEU cross section in the CNAO environment as a function of the SEU energy threshold of the electronic device under study. However, since this simplistic step-like model is not realistic, we significantly improve it by using the results of the Weibull fit of Figure 4. For each energy bin i, if P_i represents the probability per unit flux from Figure 5 and A the the cross-sectional area of the sensitive volume (1x1 μm^2), the quantity P_i/A represents the probability for a particle crossing the area A of depositing an energy larger or equal to E_i. This probability has to be weighted by the increase in the SEU cross section in that same energy interval can be evaluated from the Weibull fit as $(\sigma_{i+1} - \sigma_i)$. Therefore, the SEU cross section Σ in the neutron environment of CNAO can be derived as

$$\Sigma = \sum_i P_i \cdot (\sigma_{i+1} - \sigma_i)/A \qquad (4)$$

Assuming the neutron flux reported in [14] and considering a similar energy deposition probability as a 20 MeV proton beam, the SEU rate for TERA09 in a CNAO typical clinical treatment room is $\sim 10^2$ SEU/year. Such an upset would be easily detected, thanks to the comparison with a second independent detector (as explained in [15]). A SEU would escape the redundant control only if the data corruption would occur in the same readout cycle and in the same bit in both detectors.

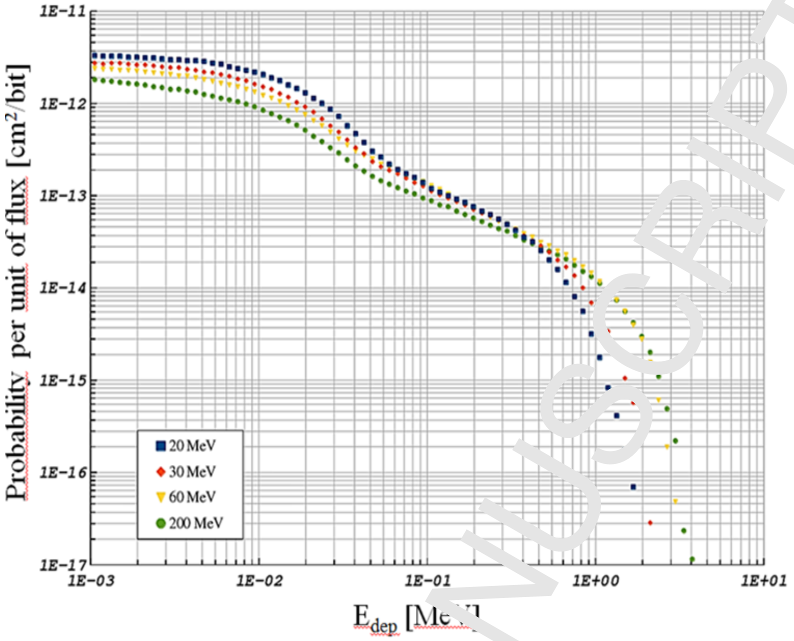

Figure 5: Energy deposition probabilities for protons of different energies. The curves show the probability to have an ionizing deposition greater or equal to the indicated E_{DEP}, within the SV. Data from [11]. The curve selected for the data analysis is the one for 20 MeV protons corresponding to the average value in Figure 6.

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From a conservative calculation, considering 1 MHz as typical CNAO monitor chamber readout frequency and a one-year-continuous data acquisition, the probability of failing the SEU detection in one readout cycle is $\sim 10^{-12}$ for each detector, i.e. $\sim 10^{-24}$ for a simultaneous upset.

Given the even larger deposited energy for the onset of SEL, compared to SEU, latch-up events are not expected to show-up in clinical applications.

7. Summary

The TERA09 ASIC is a 64 channels current to frequency converter designed in the 0.35 μm technology, to be employed as front-end readout electronics in particle therapy applications. The chip does not have embedded radiation protection techniques since it is not meant to be placed directly on beam during its activity. Nevertheless, the group was interested in characterizing the device for SEU. The test has been performed at the SIRAD Tandem accelerator at LNL in Padova, using a set of heavy ions with different energies and and target incidence angles. In this way it was possible to calculate the single event effect cross-section as a function of the deposited energy. It results that the minimum deposited energy in a CMOS silicon sensitive volume of 1 μm^3, responsible for a Single Event Upset probability higher than zero is 690 keV. Due to the fact that this ASIC will be used in

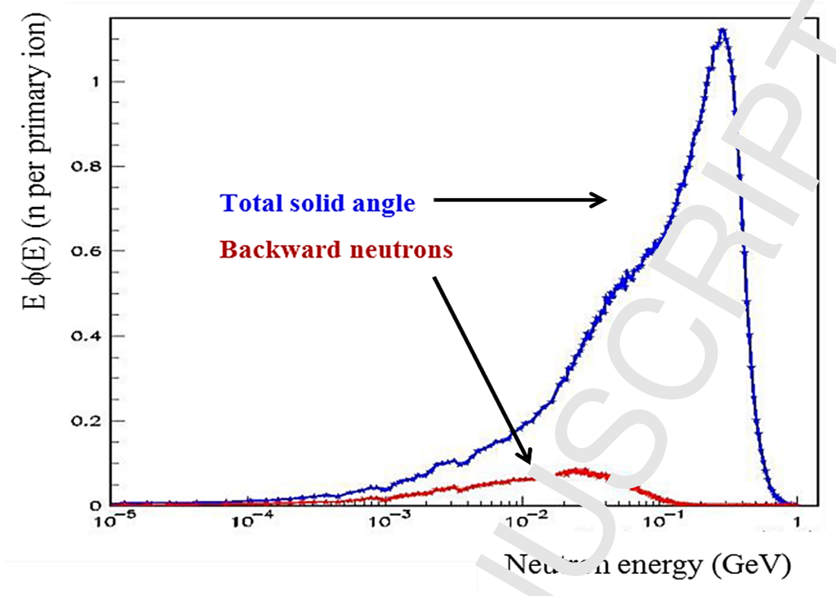

Figure 6: Spectrum of secondary neutrons produced in the backward direction by 400 MeV/u carbon ions, hitting a phantom made of ICRU tissue (International Commission on Radiation Units and Measurements); a comparison is made with the total energy spectrum of secondary neutrons.

medical applications, there was an interest in predicting the expected upset rate in a typical treatment room of CNAO. Assuming the literature data regarding the secondary neutron fluence at the CNAO nozzle and following the model developed in [11], we derived a number, $\sim 10^2$ SEU/year, which is an order of magnitude of the phenomenon.

This rate is easily controllable through redundancy, with a second independent monitor chamber already present at CNAO as in every standard clinical monitor systems. The probability to have a simultaneous bit flip in the same bit of both the monitor chambers, in a given detector readout cycle is therefore absolutely negligible (below 10^{-24} SEU/readout-cycle).

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