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1 A single ion discriminator ASIC prototype  
2 for particle therapy applications

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10 **Abstract**

11 In the framework of the development of future advanced treatment modalities in charged  
12 particle therapy, the use of silicon sensors is an appealing alternative to gas ionization  
13 chambers commonly used for beam monitoring. A prototype of a device, based on Low-Gain  
14 Avalanche Diode (LGAD) sensors with 50  $\mu\text{m}$  thickness, is being developed to discriminate  
15 and count single beam particles. This paper describes the design and characterization of  
16 ABACUS, an innovative multi-channel ASIC prototype for LGAD readout, based on a fast  
17 amplifier with self-reset capabilities. The design goals aim at detecting charge pulses in a  
18 wide range, from 4 fC to 150 fC, up to 70 MHz instantaneous rates, with a dead time of  
19 about 10 ns or less and efficiency larger than 98%. The characterization results indicate  
20 that even at the lowest input charge the signal-to-noise ratio is 15, high enough to keep full  
21 efficiency and preventing fake counts from the electronics noise. The dead time was found  
22 to be in the range between 5 ns and 10 ns, allowing to reach a full counting efficiency up to  
23 instantaneous rates of 70 MHz or larger, depending on the input charge.

24 *Keywords:* Single ion detectors, Particle therapy, ASIC design, Silicon sensors.

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## 1. Introduction

The Italian National Institute for Nuclear Physics (INFN) and the University of Torino are developing an innovative device for single ion discrimination and counting based on thin silicon detectors readout by fully custom electronics, to monitor the beam flux in proton therapy. This task is part of the INFN R&D project MoVeIT [1], an interdisciplinary collaboration involving various national research groups and the three Italian particle therapy facilities (CNAO [2], LNS [3], TIFPA [4]). MoVeIT aims at developing innovative treatment planning systems and new verification tools in radiobiology to tackle the new horizons in particle therapy, and, within this framework, the research of innovative detectors originates from the limits that the current instrumentation poses to future dose delivery strategies [5]. Indeed, the sensitivity of ionization chambers (ICs), the state-of-the-art beam monitors in charged particle therapy, limits the minimum number of particles that can be safely delivered to the order of thousands per spot, while their slow collection time (hundreds of microseconds) precludes the use of ICs on fast beam delivery strategies like, for example, volumetric rescanning and line scanning [6] to mitigate interplay effects between beam and organ motion [7]. To overcome these drawbacks, the project aims at exploring the use of thin silicon sensors ( $50\ \mu\text{m}$ ) based on the Low Gain Avalanche Diode (LGAD) design [8] with an internal gain of 10-15, achieved through a thin p+ layer implanted just beneath the n++ electrode. The signal extracted from these sensors has a well-defined shape, which amplitude is directly proportional to the internal gain, and its time duration (i.e. the charge collection time) is directly proportional to the sensor active thickness. A typical  $50\ \mu\text{m}$  thick LGAD has a charge collection time of about 1.5 ns, allowing single ion discrimination at clinical rate, and therefore well-suited to develop a particle counter for real-time beam monitoring. Moreover, to reduce the range uncertainties in particle therapy, several techniques and devices are being developed for in-vivo range verification [9] and most of them will take great advantage by the single ion discrimination capability [10].

As a proof of concept, a prototype is being developed in order to count the number of ions in an active area of  $3\times 3\ \text{cm}^2$  within 2% accuracy for radio biological instantaneous fluence rates up to  $10^8\ \text{cm}^{-2}\text{s}^{-1}$  and to measure the beam profile with a spatial resolution related to the detector segmentation (i.e. a spatial resolution of  $\sim 50\ \mu\text{m}$  for  $\sim 80\ \mu\text{m}$  wide and  $\sim 150\ \mu\text{m}$  pitch sensors).

Dedicated LGAD sensors segmented in strips and with an active thickness of  $50\ \mu\text{m}$  have been developed and produced by Fondazione Bruno Kessler (FBK, Trento) for this application. These sensors of area  $2\ \text{mm}^2$  (5pF equivalent capacitance) are designed to operate at an expected average rate per channel up to 2 MHz. Assuming a random time distribution of the particle arrival and a paralyzable model of inefficiency effects due to signal overlapping [11], the required accuracy can be achieved discriminating signals with a maximum front-end dead time of 10 ns, corresponding to a discrimination frequency up to 100 MHz for regular pulses. For a synchrotron providing a beam with a bunch structure, the design specifications refer to the average beam flux inside each bunch. In a cyclotron the maximum dead time of the system is constrained by the particle delivery, which is synchronous with the phase of the radio-frequency with a typical period of about 10 ns. Based on [12], [13], Geant4

67 simulations of energy deposit in the sensor were performed for clinical proton and carbon  
68 energies energies respectively from 60 MeV to 250 MeV and from 120 MeV/u to 400 MeV/u.  
69 This simulation results indicates that, in order to meet the required accuracy, the electronics  
70 should be efficient in detecting pulses with range of charges between 4 fC and 150 fC  
71 (adopting sensors with gain factor 1, in case of Carbon ions).

72 This paper reports on the design and the characterization of a custom front-end electronics  
73 for silicon sensors in particle therapy application. Aiming the single ion detection at clinical  
74 particle rates, the electronics requirements include nanosecond-level shaping time and high  
75 input dynamic range in charge. Concerning the use of LGAD and ABACUS with heavier  
76 ions, the energy released in the sensor would be so large ( $\sim Z^2$ ) that no internal gain would  
77 be needed to discriminate the ions while the expected lower beam flux would somehow relax  
78 the maximum counting rate requirements.

## 79 **2. Design of the front-end circuit**

80 Prior to start with a new ASIC development project, a state-of-the-art analysis was  
81 performed. Considering the field of application, beam monitoring in particle therapy is  
82 currently based on gas ionization chambers, where the advanced readout electronics is  
83 optimized for high intensity fluences [14]. Nevertheless, due to the detector features, those  
84 ASIC architectures are intended to manage average currents as input signals, without the  
85 possibility to detect the charged released by single ion interaction. In this sense, solid state  
86 detectors have several advantages in terms of speed, sensitivity and charge resolution with  
87 respect to the gas detectors. An example of nanosecond-level shaping time front-end ASIC  
88 for silicon detectors is described in [15]; although this chip is promising fast and deals  
89 with a few pF sensors, this design is tailored for SiPM readout with a  $\sim 30$  fC expected  
90 minimum charge. A few custom front-end chips for timing applications [16], [17], have  
91 been developed to readout LGADs with design and features similar to the ones adopted  
92 in the project described in this paper. Although the proper sensor-ASIC matching, these  
93 front-ends show a shaping time which is not fast enough to cope with the input signal rate  
94 expected in the application here studied. In order to deal with a dead time below 10 ns and  
95 a wide charge input range, a new custom VLSI electronics has been developed. This circuit  
96 is integrated in a 24-channels chip, nicknamed ABACUS (Asynchronous-logic-Based Analog  
97 Counter for Ultra fast Silicon strips). In order to meet the requirements, the amplifier  
98 has been designed to provide signal shaping with a few nanoseconds time duration. The  
99 design choice is based on the use of a low noise Trans-Impedance Amplifier (TIA) effective  
100 in providing signals with short rise time and on a feedback-reset circuitry used for a fast  
101 return to baseline once the input signal has been detected. Figure 1 depicts the chip layout  
102 top view. The lower part of the ASIC integrates the input pads which are packaged between  
103 grounds to better isolate the channel inputs, while the driver outputs are placed in the upper  
104 part. On the shorter edges the bias currents and the bias voltages are placed as well as the  
105 control signals. The 24 channels are symmetrically separated into two main sectors, with a  
106 central region filled with filtering capacitors.

107 The ABACUS area is  $2 \times 5 \text{ mm}^2$  and it has been designed with a commercial 110 nm

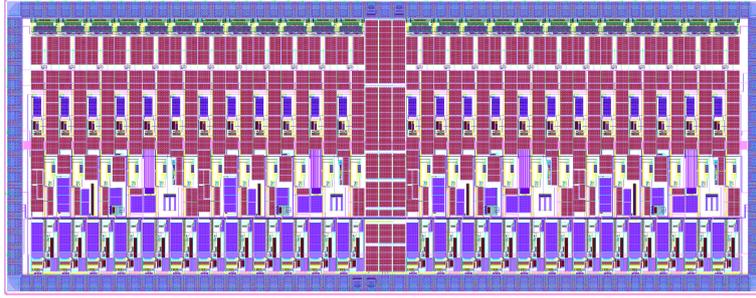


Figure 1: ABACUS layout top view. The ASIC pad-frame consists in 140 pads with 24 inputs and 48 differential outputs placed on the lower and upper long edges respectively, whereas the lateral pads are dedicated to bias and controls.

108 MOSFET technology node. The ASIC top level is arranged in four sectors with six channels  
 109 each and a sector-level bias cell, mirrored on the chip edges to mitigate possible gradients  
 110 responsible for channel-to-channel inhomogeneities. The chip will be positioned aside of the  
 111  $3 \times 3 \text{ cm}^2$  sensor at approximately 1 cm distance and will never be directly exposed to the  
 112 primary pencil beam. Considering that no digital logic is implemented, data corruption  
 113 induced by single events from scattered radiation is not a concern for this application.  
 114 Additionally, the 110 nm CMOS technology has been proven to be tolerant to ionizing  
 115 radiation up to a total dose of 50 kGy [18]. Considering an average dose of 2 Gy delivered  
 116 to a patient, 100 patients per day, 250 working days per year and assuming a very pessimistic  
 117 estimate of 10% of dose delivered to the ASIC, the chip would show no degradation due to  
 118 radiation for several years.

119 Sixty ABACUS ASICs have been taped out in an Europractice multi-project wafer.  
 120 The next subsection reports the functional level description of the ASIC channel and two  
 121 dedicated subsections provide insights into the amplifier and the feedback-reset blocks.

### 122 2.1. ABACUS channel

123 A block diagram of one ABACUS channel is shown in Figure 2. The channel can be  
 124 divided into four parts, according to their role: amplification (blocks 1 and 2), discrimination  
 125 (blocks 3 and 4), driver (blocks 5 and 6) and feedback reset (blocks 7 and 8). Standard digital  
 126 buffers have been included for signal shaping both for the long metal nets connecting the  
 127 driver and to achieve a sharp reset signal acting on the amplifier feedback capacitor (block  
 128 9).

129 The amplifier is a TIA-based design which shapes its output signal with a fast rising  
 130 edge ( $\sim 1.6 \text{ ns}$ ) while the falling edge has a long tail, depending on the product  $C_f R_f$   
 131  $\sim 18 \text{ ns}$ . Once amplified, the signal is sent to a two stages leading-edge discriminator  
 132 where it is compared with an external threshold. The pulse generated by a signal over  
 133 threshold activates a feedback reset circuitry designed for a fast return to the baseline to  
 134 prevent front-end from saturation. At the same time, the discriminator output signal is  
 135 propagated off-chip through a Current Mode Logic (CML) differential driver with a  $50 \Omega$   
 136 internal termination, selected to achieve high speed while keeping a 1.2 V common voltage  
 137 supply for the entire chip.

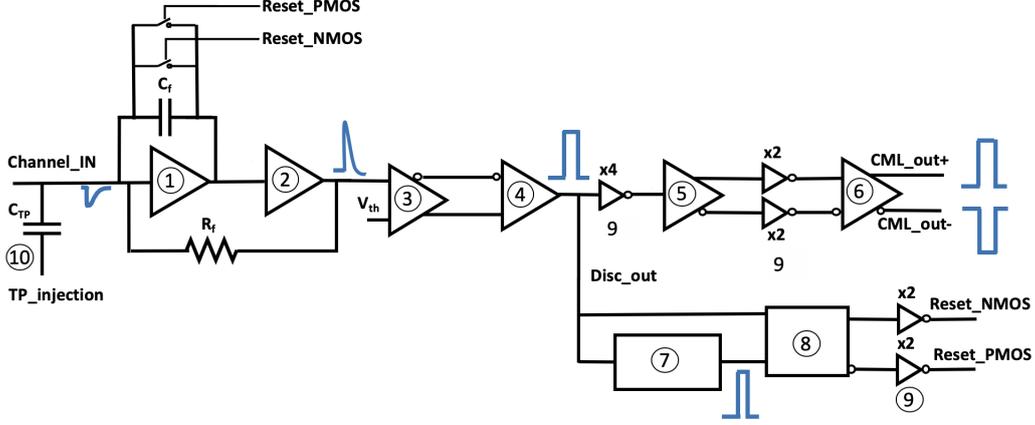


Figure 2: Block diagram of the ABACUS channel

- Charge sensitive amplifier (1), low-pass filter (2), leading edge discriminator (3,4), single ended to differential converter (5), current mode logic driver (6), pulser (7), recovery (8), inverters for signal shaping (9), test pulse circuit (10).

138 The ASIC has two integrated circuits for test-pulse injection, one connecting the even  
 139 and one the odd channels, allowing to feed an externally generated pulse through a 40 fF  
 140 test pulse capacitor ( $C_{TP}$ ).

## 141 2.2. The amplifier block

142 Figure 3 represents the block diagram of the ABACUS amplifier. The resistor feedback  
 143  $R_f$  is used to implement the TIA configuration in a two stages amplifier, where the first block  
 144 is based on a Charge Sensitive Amplifier (CSA) and the second one, an active non-inverting  
 145 low-pass filter, consists in a Operational Trans-impedance Amplifier (OTA). The CSA  
 146 has been designed implementing low noise techniques similar to other front-end amplifiers  
 147 developed for timing applications with LGADs [16].

148 The amplifier transfer function can be expressed as follows:

$$T(s) = \frac{R_f}{(1 + s\tau_r)(1 + s\tau_f)} \quad (1)$$

149 where the time constants for the TIA output voltage rising ( $\tau_r$ ) and falling ( $\tau_f$ ) edges  
 150 can be written as:

$$\tau_r \approx \frac{C_{det} \cdot (C_f + C_l)}{C_f g_{m1}} \quad (2)$$

151 and

$$\tau_f \approx \frac{C_f \cdot R_f}{(1 + R_2/R_1)} \quad (3)$$

152  
 153 In Equations 2 and 3  $C_{det}$  is the detector capacitance,  $C_f$  is the CSA feedback capacitance,

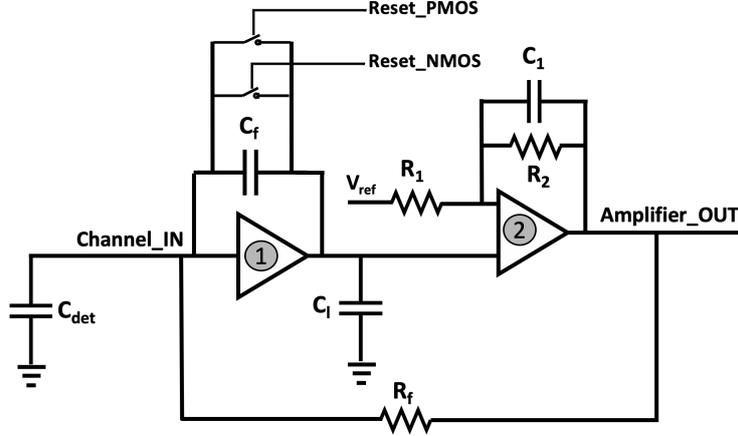


Figure 3: Block diagram representation of the ABACUS amplifier. A CSA (1) is followed by a low-pass filter (2), consisting in a OTA.

154  $C_l$  is the equivalent capacitance of the CSA load,  $g_{m1}$  is the transconductance of the CSA  
 155 input transistor,  $(1 + R_2/R_1)$  is the voltage divider at the filter input,  $V_{ref}$  is a reference  
 156 voltage used to adjust the filter operating point.

157 As reported in Equation 2, in order to compensate for the detector capacitance (5 pF),  $g_{m1}$   
 158 must be large. In addition, large  $C_f$  was chosen in order to ignore the contribution of  $C_l$ .  
 159 To meet these requirements, a large bias current of  $\sim 8$  mA and a feedback capacitance of  
 160 500 fF have been set for the CSA. The  $R_2/R_1$  ratio has been chosen larger than 1 to achieve  
 161 additional gain. For the feedback resistance  $R_f$ , a value of 35 k $\Omega$  has been chosen in order  
 162 to keep the noise low, provide a sufficient low-frequencies gain, while contributing for the  
 163 signal shaping and for the amplifier stability. The amplifier output amplitude depends on  
 164 the effects of both the CSA and the filter. Operating on  $V_{ref}$ , it is possible to use the filter  
 165 to attenuate the signal for measurements of a wide range of input charges. Although from  
 166 simulation the conversion factor can be adjusted up to 2.5 mV/fC, the nominal setting is  
 167 obtained with the filter gain at  $\sim 1$ , resulting in a 1.21 mV/fC overall conversion factor.  
 168 Figure 4 shows the amplifier output amplitude as a function of the input charge, in the  
 169 nominal operating condition. The amplifier behaves linearly up to 120 fC, where it starts  
 170 saturating. From transient noise simulations, the expected rms noise of the entire amplifier  
 171 is found to be 0.47 mV.

### 172 2.2.1. The Charge Sensitive Amplifier

173 The adopted LGADs provide negative currents and this lead to the choice of a single  
 174 polarity front-end design. An additional reason for choosing single polarity stages is related  
 175 to a better noise figure, improving the discrimination efficiency at high rates and low charges.  
 176 In Figure 5 the transistor-level schematic representation of the ABACUS CSA is shown. The  
 177 CSA topology consists of a NMOS input telescopic cascode with two independent branches.

178 The open loop gain is given by the product between the NM1 transconductance and  
 179 the drain-source resistance of the cascoding device. A second independent branch is used

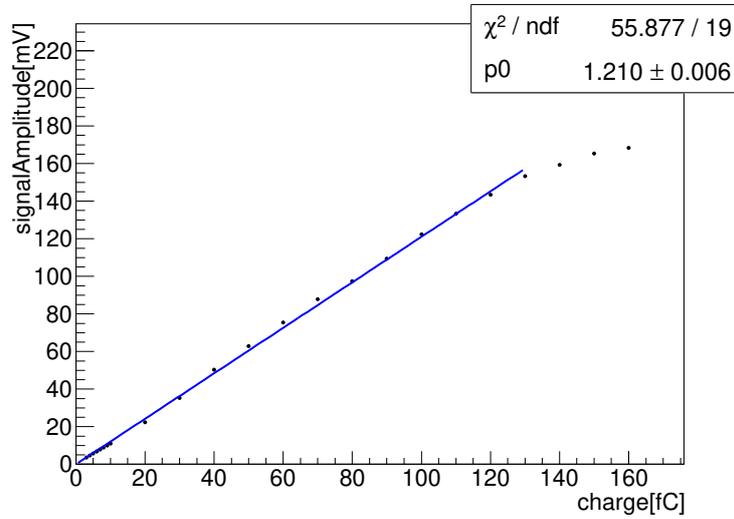


Figure 4: Amplifier linearity simulation results.  $p0$  is the fit slope, representing the charge-to-signal-amplitude conversion factor.

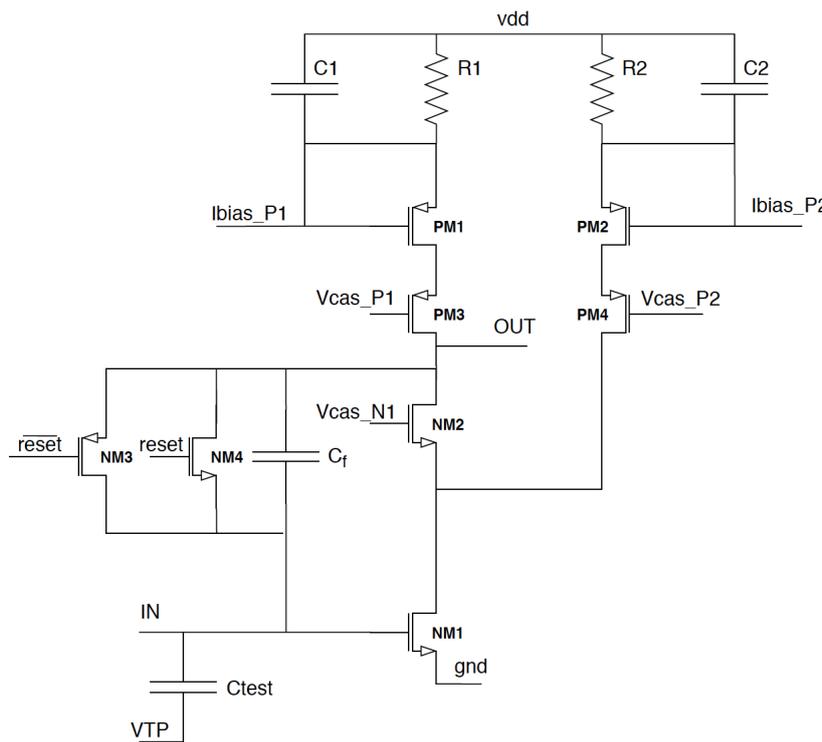


Figure 5: Schematic representation of the ABACUS charge sensitive amplifier.

180 to increase the open-loop gain. The left branch biases the cascodes PM3 and NM2 with  
 181  $\sim 200\mu\text{A}$  current; increasing this current, the output voltage slew rate increases but at the  
 182 same time the swing decreases. The second branch of the CSA (transistors PM2 and PM4)

183 is used to provide to the input transistor the largest part of its current ( $\sim 8$  mA).

### 184 2.3. The feedback-reset circuitry

185 The feedback reset occurs at channel level and each channel operates on his own capacitor,  
 186 activating and managing this functionality independently from the others. The amplifier  
 187 RC components in the feedback connection would result in a long tail that would limit the  
 188 efficiency at large repetition rates. This effect has been mitigated by using the feedback-reset  
 189 circuitry, which includes the sequential action of a pulse generator and a recovery system to  
 190 activate the switching capacitor MOSFETs and reset the CSA feedback capacitor.

#### 191 2.3.1. Pulse generator

192 The CSA feedback capacitor reset is performed by a block called "pulser". Referring to  
 193 Figure 6, the discriminator output is inverted (line S1) and then is inverted again using a  
 194 starved inverter to introduce a delay (line S2); finally a third inverter digitizes again the  
 195 delayed signal (delayed\_IN). This delayed signal is fed into a boolean AND gate with the  
 196 original discriminator output. This allows to have a pulse that starts as close as possible in  
 197 time to the discriminator output (1.2 ns, independently of the signal amplitude), lasting for  
 198 a short time set by the RC delays of the inverters. Moreover, it is possible to change the  
 199 pulse duration from a minimum of 0.4 ns to a maximum of 2 ns, operating with two bias  
 200 voltages controlling the second inverter delay (PulserVbiasP, PulserVbiasN).

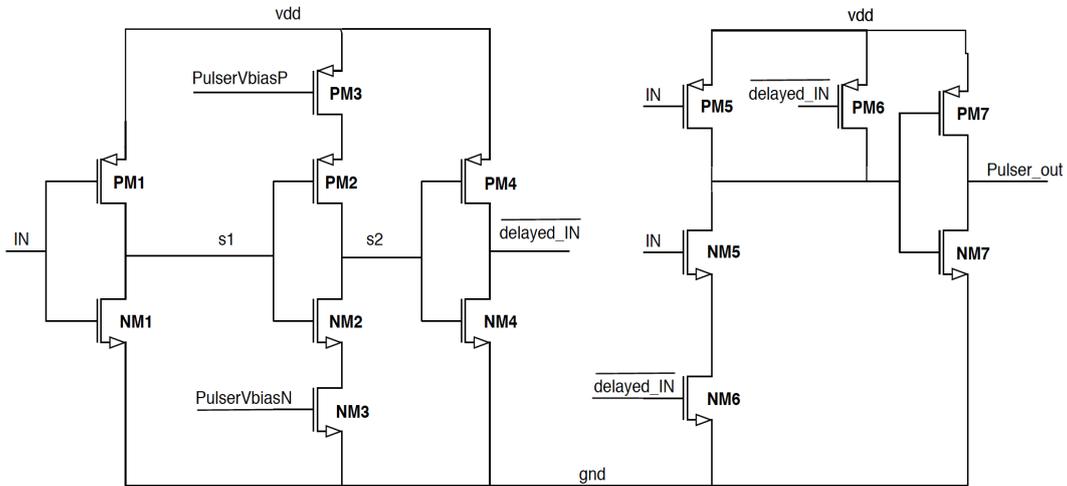


Figure 6: Pulser: transistor level representation. The output signal results from a boolean AND between the input and a delayed and inverted copy of the input. The two signals overlapping duration can be varied with the PulserVbiasP and PulserVbiasN voltages.

#### 201 2.3.2. Recovery system

202 The Pulser action is designed to reset as fast as possible the amplifier output voltage to  
 203 the baseline with the minimum possible deadtime. However, in situations characterized by  
 204 high signal rates, the duration of the reset signal of the pulser could not be long enough

205 to bring the front-end signal below threshold, leading to the discriminator remaining fixed  
206 in a stuck condition. To avoid this effect, a circuit named "recovery" has been added.  
207 The recovery output signal is used to control an NMOS switch-reset transistor for resetting  
208 the amplifier feedback, whereas its negated signal is used to control a PMOS switch reset  
209 transistor adopted for the collection of the charge injection due to the NMOS switching.  
210 The working principle of the recovery block is based on a boolean OR between the pulser  
211 output and the discriminator output signals, the latter overtaking a high-pass filter with  
212 time constant  $\tau = 3.5$  ns. In normal conditions the discriminator output is reset by the  
213 pulser signal well before  $\tau$ . When the discriminator output is still high after  $\tau$ , the recovery  
214 circuit generates a second longer reset pulse to the front-end which forces the restore of  
215 baseline.

### 216 3. ABACUS characterization

217 The ABACUS ASIC has been tested in laboratory to check its performance in terms of  
218 electronics noise, amplifier baseline stability and gain. The ASIC measured power consumption  
219 is  $\sim 30$  mW/ch and the main part of this power is equally shared between the amplifier and  
220 the driver. It is worth to mention that the power budget was not a design constraint  
221 whereas the single ion discrimination capability over a wide charge and frequency range is  
222 the ABACUS figure of merit. This point has been stressed during the tests.

#### 223 3.1. Setup and methodology

224 A custom board for testing the ASIC has been developed integrating trimmers for  
225 currents and voltages settings, as well as a 16-bits DAC for remote setting of the discriminator  
226 threshold voltage. An FPGA was used to readout and control the ASIC, while the input  
227 signal has been provided by means of a voltage pulse source connected to the channel input  
228 through a capacitor. Two variants of this setup have been used, one based on the integrated  
229 test pulse circuit and a second one using an external capacitor connected to the input pad  
230 of a single channel. For the setup based on the integrated capacitors, the pulse injection  
231 has been provided using an external pulser unit Active Technologies Pulse Rider PG-1072).  
232 In Figure 7, an oscilloscope screen-shot shows one polarity of the output differential signal  
233 (CML\_out+) and the input from the pulser (Pulse\_A), for 33 fC charge pulses with 125  
234 MHz repetition rate. The delay between the falling edge of the pulser signal and the ASIC  
235 output pulse is  $\sim 5 - 6$  ns, for a 33 fC injected charge, and is due to the intrinsic delays of the  
236 amplifier and the discriminator blocks and to the R-C contributions from layout parasitic  
237 effects.

238 This configuration has the intrinsic limitation in the maximum injected charge of 48  
239 fC, due to the maximum voltage of 1.2 V that can be injected through the 40 fF internal  
240 capacitance. Furthermore, for each voltage pulse two input charges of opposite polarities  
241 are injected into the channel. Since the reset circuit is not activated with a positive input  
242 charge, this would lead to a drift of the baseline especially at large input frequencies. A  
243 second setup based on a 500 fF external capacitor and uni-polar voltage input steps has  
244 been used. An external board (LTC200IY-2303A) based on a 16-bit high speed DAC with

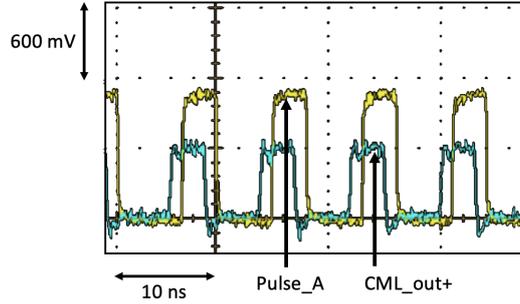


Figure 7: Oscilloscope screenshot with pulser-injected input signal (yellow) and the CML driver output signal (light blue), corresponding to a 33 fC injected charge and pulse frequency of 125 MHz. The driver output results from the falling edge of the injected pulse.

245 300 mV voltage swing and 2.2 GHz bandwidth was implemented to provide a voltage ramp  
 246 with programmable step height and frequency. A LabVIEW control program was used to  
 247 configure the ramp cycle selecting the number of steps, their duration and the ramp plateau  
 248 width. In order to avoid instabilities of the amplifier, a slow falling ramp was implemented  
 249 using small voltage steps. Figure 8 shows an oscilloscope screenshot with 10 voltage steps  
 250 separated by 100 ns, together with the positive polarity output of ABACUS.

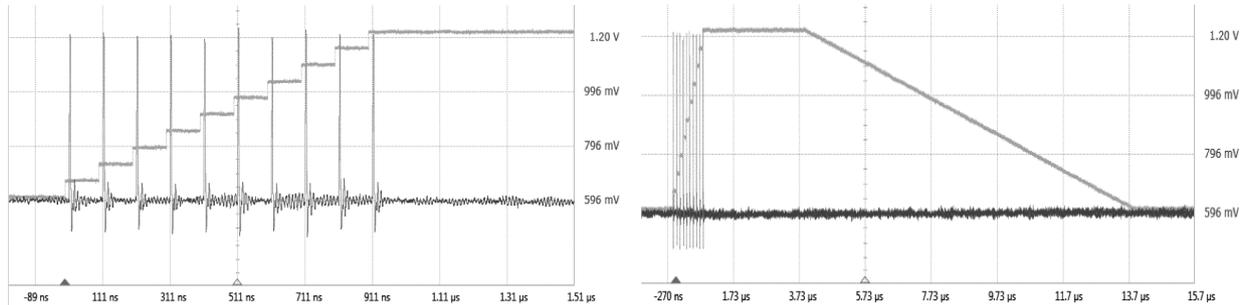


Figure 8: Left: 10 steps voltage ramp with a 100 ns step-separation and the ABACUS driver output signal (CML\_out+). Right: the complete ramp cycle, composed by the voltage steps, the plateau and the slow falling tail.

251 In both setups, the ABACUS differential outputs have been readout by an FPGA board  
 252 (Xilinx Kintex7-Ultrascale XCKU040), sampling the outputs at 1 GHz and counting the  
 253 number of 0-1 transitions. The same FPGA has been used to control the discrimination  
 254 threshold by operating the 16-bit on board DAC. A LabVIEW program was prepared to  
 255 acquire the counting rate and to setup runs increasing the threshold in small steps during  
 256 the acquisition. An example of results for 30 fC pulses injected at 10 MHz is shown in the  
 257 left side of Figure 9; the counting efficiency, defined as the ratio of counting rate over the  
 258 input pulse rate, is here shown as a function of the threshold. Similar runs were performed  
 259 with different pulse frequencies up to 130 MHz for both the setups. More in detail, charges  
 260 ranging between 3 fC and 20 fC were injected into the 40 fF integrated capacitor whereas  
 261 the the external 500 fF test pulse capacitor was used for the 30 fC-160 fC range. Increasing

262 the threshold, the counting efficiency moves from large values around the baseline level,  
 263 where the noise induces high frequency of counts, to a flat plateau where the signal is  
 264 discriminated with full efficiency. When the threshold reaches the signal peak, the counting  
 265 efficiency drops to 0, as shown in the right panel of Figure 9, with a slope caused by the  
 266 electronics noise which overlaps with the signal.

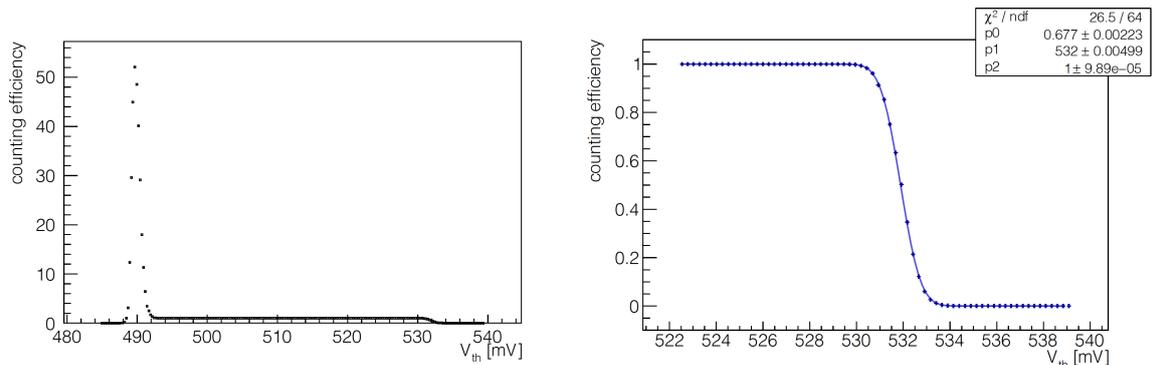


Figure 9: Left: example of a discriminator voltage threshold scan for a 30 fC signal injected into the chip test pulse pad with 10 MHz repetition rate. Right: expanded view of the threshold axis, where the counting efficiency drops from 1 to 0. The p0 parameter represents the noise standard deviation expressed in mV whereas the p1 parameter is the voltage threshold at which the efficiency is equal to 0.5. The p2 fit parameter represents the efficiency normalization factor.

267 In order to fit the points, a convolution of a step function with a gaussian (sigmoid fit)  
 268 has been used to extract the signal amplitude corresponding to the threshold voltage at  
 269 0.5 efficiency (p1 fit parameter) and the standard deviation of the electronic noise (p0  
 270 fit parameter):

$$f(x) = p_2 \int_x^{+\infty} 1/(\sqrt{2\pi p_0^2}) e^{-(x-p_1)/2p_0^2} dx' \quad (4)$$

271 where  $x$  is the voltage threshold and  $p_2$  is a parameter adopted for data normalization.

### 272 3.2. Results

273 The amplitude of the amplifier output has been estimated with the threshold scan  
 274 described before, as a function of the injected charge and pulse frequency. A configuration  
 275 reproducing the conversion factor of Figure 4 has been adopted for this test. For small  
 276 charges up to 20 fC the integrated 40 fF capacitor was used (Figure 10, left), while for large  
 277 charges the pulses were injected into the external 500 fF capacitor to extend the charge  
 278 range up to 160 fC (Figure 10, right).

279 In both the figures, the signal amplitudes measured with 1 MHz pulse frequency have  
 280 been reported after the subtraction of the baseline value, defined as the linear fit intercept.

281 The measured conversion factor (the p0 parameter in Figure 10) for the setup based  
 282 on the external capacitor is compatible with the expectation from the simulation results  
 283 reported in Figure 4. The left plot of Figure 10 is related to the internal test capacitor and

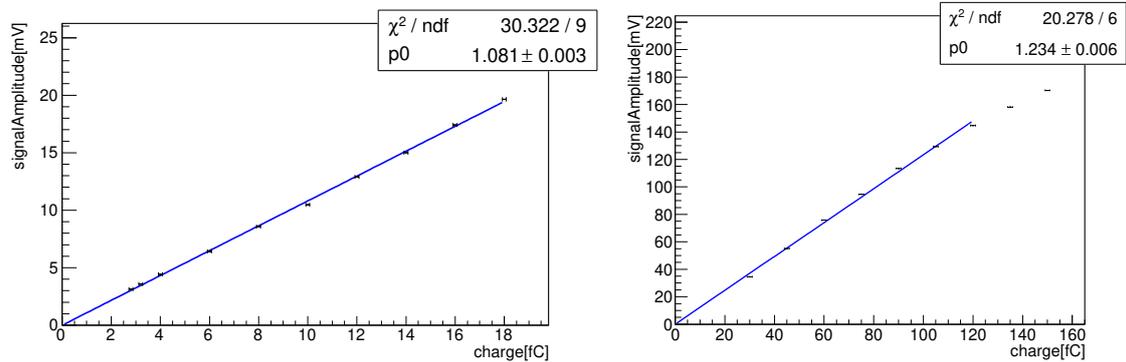


Figure 10: Amplitude of the amplifier output signal as a function of the charge injected at 1 MHz rate through the integrated 40 fF capacitor (left) or the external 500 fF capacitor (right).

284 the pulser-based setup; in this case the pulser rising time ( $\tau_r$ ) is fixed by the instrument  
 285 constraints to 200 ps whereas the DAC-based setup has a 1 ns  $\tau_r$ . Since the ABACUS  
 286 amplifier has been designed with a bandwidth tailored to deal with LGADs with a typical  
 287 charge collection time of 1 ns, faster signals result in lower amplification. For both the  
 288 charge ranges the counting efficiency is 100% and the amplifier output is linear with the  
 289 input charge, up to 120 fC where the amplifier saturation starts to occur.

290 Figure 11 shows the noise standard deviation determined by the sigmoid fit described earlier  
 291 as a function of the charge injected at 1 MHz through the 40 fF internal capacitor (red  
 292 markers) and through the 500 fF external capacitor (black markers).

293 The results indicate that the electronics noise is independent on the injected charge, for each  
 294 set of measurements. The data collected operating with the integrated test capacitor are  
 295 within  $\pm 0.05$  mV the electronics noise value obtained from circuit simulation (0.47 mV).  
 296 This kind of shift is compatible with what was expected during the design phase, due to  
 297 simulation approximations. The higher noise level measured using the external capacitor is  
 298 related to parasitic effects due to the longer injection path. The test has been repeated at  
 299 different repetition rates with no effect on the measured values.

300 In order to study the dead time of the discrimination circuitry, the efficiency in separating  
 301 two consecutive input pulses is measured as a function of their time delay. The 2-pulses set  
 302 repetition rate was fixed at 10 KHz in order to avoid the high-frequency continuous pulse  
 303 effects, discussed afterwards as dedicated test results. The results are shown in Figure 12  
 304 for different input charges. A full 2-pulses detection efficiency is achieved with time delays  
 305 greater than 10 ns while a drop in the efficiency appears at lower time delays depending  
 306 on the input charge. Two different effects degrade the discrimination efficiency: for low  
 307 charges, e.g. 6 fC, the signal-to-noise-ratio (SNR) is low and the discriminator could miss  
 308 the signal detection whereas for very large charges, e.g. 100 or 150 fC, the amplifier return  
 309 to baseline time is more affected by the larger signal amplitude. Therefore, the two effects  
 310 are correlated because maximizing the SNR was not adopted as design solution since it  
 311 would lead to either amplifier saturation or low discrimination frequency. The best result is  
 312 achieved for 50 fC injected pulses.

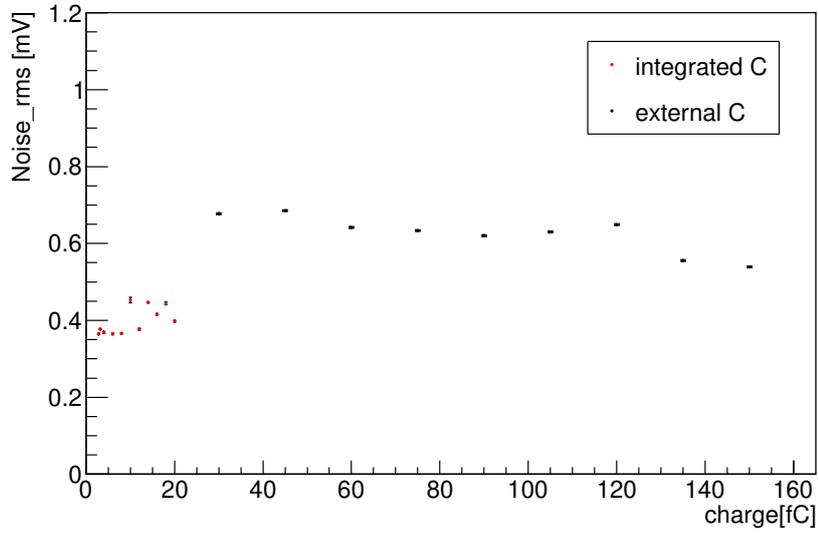


Figure 11: ABACUS noise standard deviation a function of the charge injected either into the 40 fF internal capacitance (red markers) or into the 500 fF external capacitance (black markers).

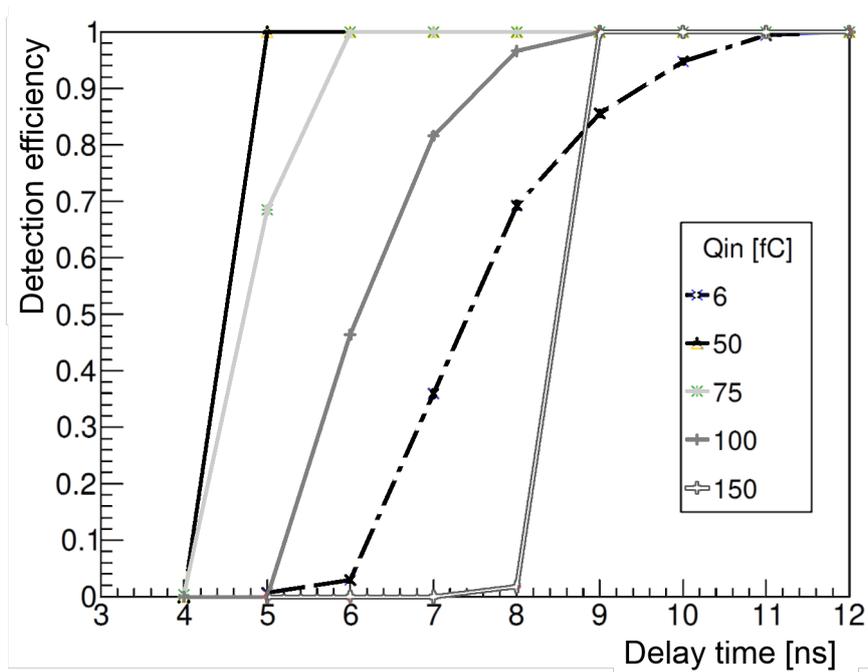


Figure 12: 2-pulse detection efficiency as a function of the time delay, for different injected charges.

313 The counting efficiency has been measured fixing both the input charge and the discriminator  
 314 threshold while changing the signal repetition rate. This setup is based on the high speed  
 315 DAC board, described in the previous section, providing configurable voltage ramps and

316 repeating the ramp cycle 100 times. Figure 13 reports the results for two injected charge  
 317 pulses, 20 fC and 4 fC. For the 20 fC charge, increasing the signal repetition rate the counting  
 318 efficiency remains higher than 99% up to 110 MHz, while for the lower charge the drop in  
 319 efficiency starts at lower repetition rates. This behaviour is compatible with the higher dead  
 320 time found at low charges.

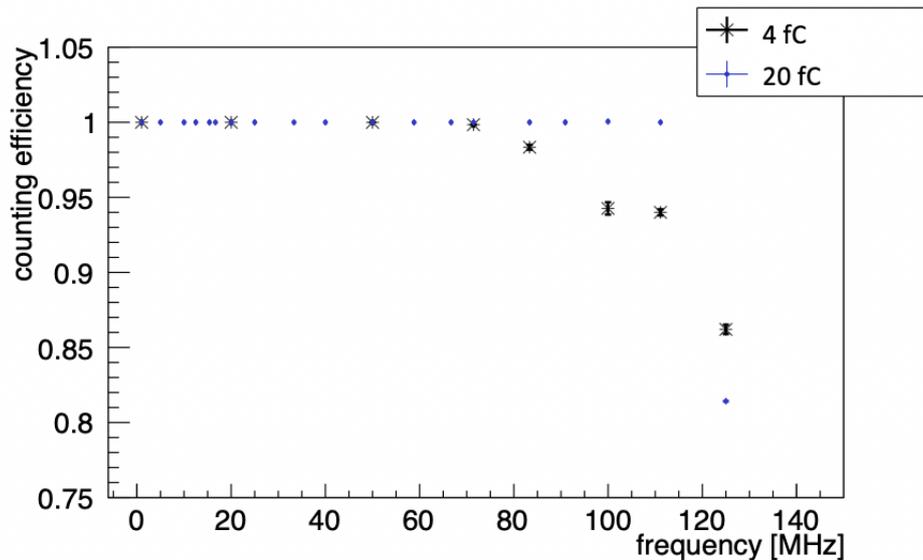


Figure 13: Counting efficiency vs frequency of the injected signal for 20 fC and 4 fC signal amplitudes. The signals are provided by the high speed DAC circuit board and the discriminator threshold has been fixed 3 mV above the electronics noise.

#### 321 4. Discussion

322 The precise measurement of the delivered dose in particle therapy is a challenging task  
 323 that relies on the precision and stability of the beam monitoring system. The reference  
 324 detectors used since many decades are based on gas ionization chambers which offer several  
 325 advantages in terms of simplicity, robustness, ease of operation and minimal perturbation  
 326 of the beam. However, their sensitivity is limited to  $O(10^3)$  protons [19], while the charge  
 327 collection time can be as large as hundreds of  $\mu s$ . These drawbacks prevent their use in  
 328 emerging new dose delivery modalities aiming to mitigate uncertainties due to organ motion  
 329 [7], like volumetric rescanning and line scanning [6], where faster beam movements and small  
 330 doses need to be accurately monitored.

331 These drawbacks prevent their use in emerging new delivery modalities where faster  
 332 beam movements and small doses need to be accurately monitored. As an alternative,  
 333 solid state detectors offer sensitivity to single ions that could change the paradigm used for  
 334 monitoring the beam flux from an integrated charge measurement to single ion counting.  
 335 The direct measurement of the number of protons would not rely on accurate dosimetric

336 calibrations and on the beam particle energy. Recent developments of thin LGAD sensors  
337 allow to achieve very short signal duration with similar signal-to-noise ratio as traditional  
338 thicker silicon sensors. This, combined with fine sensor segmentation aimed to reduce the  
339 expected particle rate for each channel, would allow to count particles at the large fluxes of  
340 therapeutic beams.

341 The clinical constraint of counting efficiency better than 98% requires a very fast dedicated  
342 front-end readout able to detect pulses with the large range of charges expected for protons of  
343 different energies (from 60 to 250 MeV) in 50  $\mu\text{m}$  silicon thickness. The minimum measured  
344 SNR of 15 demonstrates the capability of separating signals from the electronic noise even at  
345 the smallest input charge of 4 fC. Given the random time distribution of particle arrival, the  
346 overlap of signals is the limiting factor in the maximum achievable counting rate. Therefore,  
347 the dead time introduced by the electronics must be reduced as much as possible. The results  
348 obtained in terms of two pulse detection efficiency indicates that the dead time is always  
349 smaller than 10 ns for all the injected charges except for the 6 fC charge, where the detection  
350 efficiency is still larger than 95%. This effect is addressed to the fact that the low-charges  
351 are provided by the pulser with a pulse rising time not ideal for the ABACUS amplifier  
352 bandwidth, as explained discussing the 2-pulses detection efficiency results. Moreover, the  
353 low-charge discrimination is more affected by leakage or parasitics due to the fact that the  
354 pulse is not directly injected into the front-end amplifier but moves through the test pulse  
355 injection circuit, shared among several channels (all the even or all the odds channels). This  
356 result guarantees, with the current design of strip segmented LGADs, the measurement  
357 of a flux of  $10^8 \text{ cm}^{-2} \text{ s}^{-1}$  with 2% accuracy for a beam provided by a cyclotron or for  
358 a continuous beam. Bunched beam from synchrotron of similar average flux could suffer  
359 for larger inefficiencies due to larger instantaneous particle rates in each bunch and would  
360 require smaller strip or pixel size.

## 361 5. Conclusions

362 A novel custom front-end ASIC for single ion detection in particle therapy applications  
363 has been developed. It integrates in a single chip 24 channels, designed with a trans-impedance  
364 amplifier followed by a discriminator with adjustable threshold. Particular care was devoted  
365 to the design of a fast baseline restore mechanism to achieve low dead time capability.  
366 A laboratory setup was prepared for the characterization which allows to inject pulses of  
367 different charges and frequencies. A FPGA-based readout system allows to count the pulses  
368 detected by the chip and to set values of the discriminator threshold. Threshold scans at  
369 fixed input charge and frequency were used to determine the amplitude of the amplifier  
370 output, as well as the noise. The results show good linearity of the amplifier for the range of  
371 charges expected for the envisaged application, with a gain compatible with the simulations.  
372 The low noise level, charge independent, lead to a signal-to-noise ratio larger than 10 even  
373 at the smallest input charges. The dead time was estimated by studying the efficiency in  
374 detecting two input pulses as a function of their time delay. The results indicate that a  
375 dead time smaller than 10 ns can be achieved for input charges larger than 6 fC. Finally,  
376 the fraction of detected pulses was measured as a function of the pulse rate, showing that

377 100% efficiency is achieved up to over 100 MHz for all the input charges but for 4 fC, where  
378 the efficiency starts to drop at 70 MHz. Therefore, the reported results demonstrate that  
379 the developed ASIC is compliant with the MoVeIT requests, as it is able to detect charge  
380 pulses in the range 4-150 fC up to 70 MHz instantaneous rate, with a dead time of about  
381 10 ns or less and efficiency larger than 98%.

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385 L.232/2016, art.1, cc. 314, 337).

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