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Full Length Article

Digital pixel test structures implemented in a 65 nm CMOS process

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ABSTRACT

The ALICE ITS3 (Inner Tracking System 3) upgrade project and the CERN EP R&D on monolithic pixel sensors are investigating the feasibility of the Tower Partners Semiconductor Co. 65 nm process for use in the next generation of vertex detectors. The ITS3 aims to employ wafer-scale Monolithic Active Pixel Sensors thinned down to 20–40 μm and bent to form truly cylindrical half barrels. Among the first critical steps towards the realisation of this detector is to validate the sensor technology through extensive characterisation both in the laboratory and with in-beam measurements. The Digital Pixel Test Structure (DPTS) is one of the prototypes produced in the first sensor submission in this technology and has undergone a systematic measurement campaign whose details are presented in this article.

The results confirm the goals of detection efficiency and non-ionising and ionising radiation hardness up to the expected levels for ALICE ITS3 and also demonstrate operation at +20 °C and a detection efficiency of 99%

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for a DPTS irradiated with a dose of 10^{15} 1 MeV n_{eq} cm^{-2}. Furthermore, spatial, timing and energy resolutions were measured at various settings and irradiation levels.

1. Introduction

Over the past decade, Monolithic Active Pixel Sensors (MAPS) have well established their position in high energy physics experiment vertex detectors [1–3]. By combining the readout circuitry and the sensitive volume in the same sensor produced in commercial processes, they pave the way for ultra-thin and large-scale tracking detectors. The state-of-art ALPIDE chip, in use in the ALICE Inner Tracking System 2 (ITS2), was produced in the TowerJazz 180 nm technology and demonstrated an excellent detection efficiency (≫99%) and spatial resolution (5 μm) performance at very low power dissipation (<40 mW/cm^2) and material budget of 0.05%X/X_0 up to irradiation levels of about 3 kGy and 10^{13} 1 MeV n_{eq} cm^{-2} [4–6]. Other developments produced in the same technology demonstrated comparable detection efficiency at −20 °C even after a non-ionising radiation dose of 10^{15} 1 MeV n_{eq} cm^{-2} [7]. The next upgrade of ALICE tracker, the ALICE ITS3, planned for the Long Shutdowns 3 (2026–2028), is extending the requirements on the sensor characteristics. The ITS3 detector integration imposes a wafer-scale sensor size $O(10 \times 27\,cm^2)$ and operation at temperatures achievable by air cooling $O(+20\,°C)$ [8].

In order to address the arising challenges in the design of the next generation MAPS detector, the Tower Partners Semiconductor Co. (TPSCo) 65 nm CMOS imaging process [9] was chosen as the starting point in the framework of the ALICE ITS3 upgrade [8,10] and the CERN EP R&D on monolithic pixel sensors [11]. The critical aspect of the new technology node for the ALICE ITS3 is the larger wafer size (30 cm as opposed to 20 cm in TowerJazz 180 nm process). The goal of the first submission designated MLR1 and produced in summer 2021, was to verify the radiation hardness (the expected levels for the ITS3 are below 10^{13} 1 MeV n_{eq} cm^{-2} and 10 kGy [8]) and the detection efficiency (>99%) of the MAPS produced in this technology. Therefore, a sensor prototype featuring in-pixel amplification and discrimination was characterised using soft X-rays and ionising particle beams and the results are described in this paper. In particular, the sensors were irradiated[1] up to 100 kGy and 10^{15} 1 MeV n_{eq} cm^{-2} and their detection efficiency and spatial, timing and energy resolutions were measured. In total, 48 sensors have been tested, with at least two for each radiation level (three in case of 10^{15} 1 MeV n_{eq} cm^{-2}). For visualisation purposes and to eliminate any selection bias, each measurement point is represented by a single device, chosen as the first one that was tested.

[1] Sensors irradiated with non-ionising, ionising, and combined doses were exposed to neutrons at JSI Ljubljana, 10 keV X-rays from a tungsten target at CERN, and 30 MeV protons at NPI Prague, respectively.

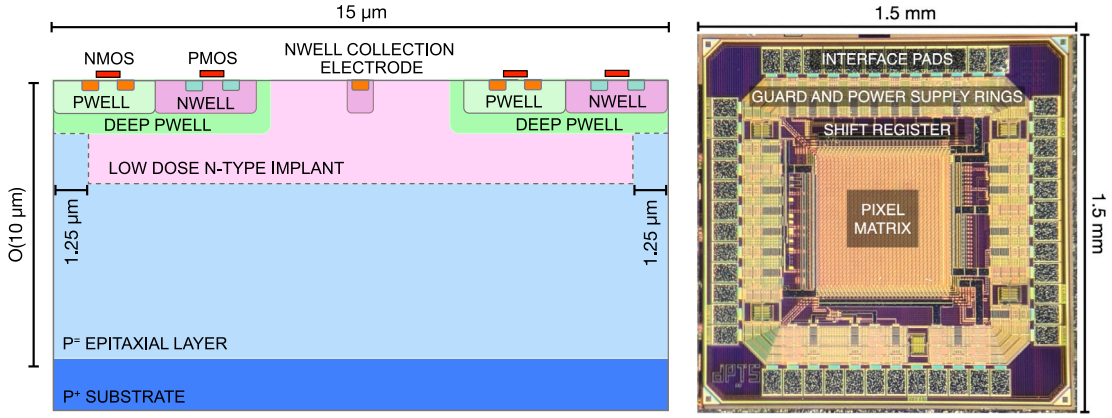
2. The DPTS chip

The Digital Pixel Test Structure (DPTS) is the most complex prototype MAPS produced in the first submission in TPSCo 65 nm technology process [9]. In order to optimise the technology for ionising particle detection, the submission was produced in four process splits, gradually modifying the doping levels of various implants (cf. Fig. 1(a)). The present work focuses only on the split expected to yield the best performance [12].

To better collect the signal charge and accelerate it to the collection diode, similar measures to those in the 180 nm technology have been applied [7,13]. As illustrated in Fig. 1(a), a deep, low-dose, *n*-type implant has been introduced to displace the junction from the collection diode into the epitaxial layer and thus deplete the epitaxial layer over the full pixel width [13]. This additional implant does not extend to the pixel border, but there is a gap in the implant near the pixel edges with the aim to increase the lateral field, pushing the signal charge to the collection diode [14]. This is expected not only to accelerate the charge collection but also to reduce charge sharing to give more operating margin due to the larger seed pixel signal.

The DPTS chip (cf. Fig. 1(b)) measures 1.5 mm × 1.5 mm and features a 32 × 32 pixel matrix of 15 μm × 15 μm pitch, controlled by a set of external reference currents and voltages, and read out via a current mode logic (CML) output. The in-pixel front end amplifies, shapes, and discriminates the signal from the collection diode. The positions of the hit pixels are time-encoded (cf. Section 2.2) and all 1024 pixels are read out simultaneously via a differential digital output line (cf. Fig. 2). The pixels can be masked from readout and selected for pulsing via a 480 bit triplicated shift register. Given its space-constrained size, the possible masking and pulsing combinations are limited. Those used in this paper are the following: pulsing a single pixel, masking a single pixel, and masking the whole matrix with the exception of one row (unmasking a single pixel is not possible).

Fig. 1(b) shows a photograph of the DPTS taken under a microscope. Starting from the centre and going outwards, the pixel matrix, shift register block, guard rings, and bonding pads can be distinguished. Most of the pads are dedicated to supplying power and reverse bias to the chip. The power supply is split into three domains (all operated at +1.2 V):



(a) Pixel cross section. Not to scale.

(b) Chip under microscope.

Fig. 1. A cross section of a DPTS pixel and a photo of the chip under a microscope.

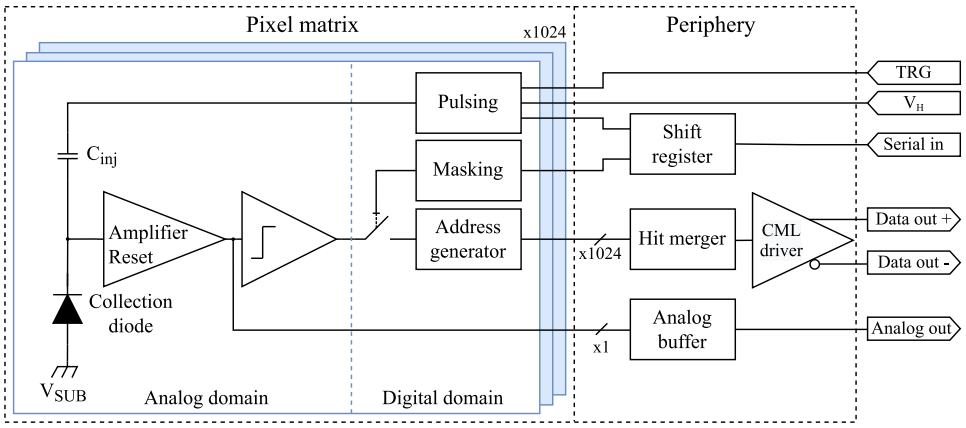


Fig. 2. DPTS functional diagram. 1024 pixels can be masked from readout and selected for pulsing via a shift register. The addresses of hit pixels are read out via a differential digital output line. The in-pixel amplifier output of a single pixel is connected to an interface pad.

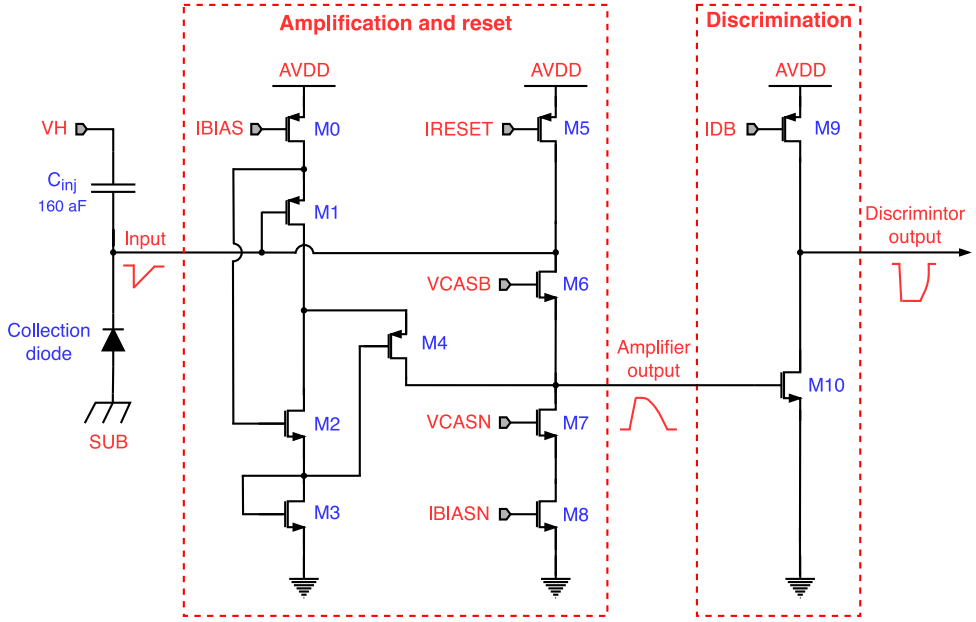


Fig. 3. In-pixel amplifying, discriminating and reset circuit. All front-end biases are provided externally, in common to all pixels.

analogue in-pixel front end, CML output driver, and all other digital circuitry. The reverse bias can be supplied separately to the substrate (V_{sub}) and the deep p-wells (V_{pwell}) hosting the circuitry (cf. Fig. 1(a)), however, in this work they were kept at the same potential.

There are three variants of the chip, implementing different time-encoding (cf. Section 2.2) and ground connection schemes.[2] As the laboratory testing revealed no difference in their performance, no distinction will be made in the results discussed here.

2.1. In-pixel front end

The analogue in-pixel front-end circuit (cf. Fig. 3) is controlled via four currents (I_{bias}, I_{biasn}, I_{reset} and I_{db}) and two voltages (V_{casb} and V_{casn}), all externally generated and supplied to the chip via the interface pads. The front end [15] is based on a high gain cascoded inverting amplifier, requiring direct feedback to the input to correctly define its operating point. This is achieved by the V_{casb} transistor (M6) in combination with the I_{reset} current source (M5): the feedback will make the current through the V_{casb} transistor equal to I_{reset} minus the leakage current on the collection electrode and correctly set the voltage of the collection electrode. When charge is collected on the collection diode, the output of the inverting amplifier at the source of the V_{casb} transistor will make a positive voltage excursion and switch off the V_{casb} transistor, causing the collection diode to be reset by a constant current and, therefore, resulting in a close to linear time-over-threshold behaviour. The high gain amplifier output is the input to a subsequent common-source stage (M9–M10). As soon as the amplifier output is sufficiently high for the input transistor of this second stage to overcome I_{db}, the output node of the second branch will fall and convert the signal into a digital rail-to-rail signal.

The front end has been designed to operate at current levels in the main branch (I_{bias}, M0–M3) between 10 nA and 5 µA, in a power-to-speed trade-off. The I_{biasn} current source (M8) balances the amplifier output current and is to be operated at one-tenth of the I_{bias} current. V_{casn} (M7) is used to further control the operating margin of the amplifier. In the lower current ranges, all transistors are in weak inversion. In addition, the NMOS transistors are subject to the reverse bias applied to the sensor (V_{pwell}), requiring biases like V_{casb} and V_{casn} to be adjusted to

[2] In one of the DPTS variants, the ground of the digital and analogue power domains is connected on the chip. In all the measurements presented in this paper, the ground was connected for all three power domains off-chip.

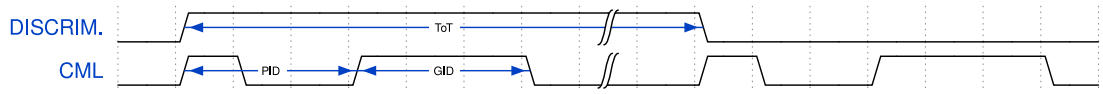


Fig. 4. DPTS hit position encoding scheme. The two pulses encoding the pixel position with the matrix are sent to CML output, both at the assertion and at the deassertion of the discriminated pixel output signal.

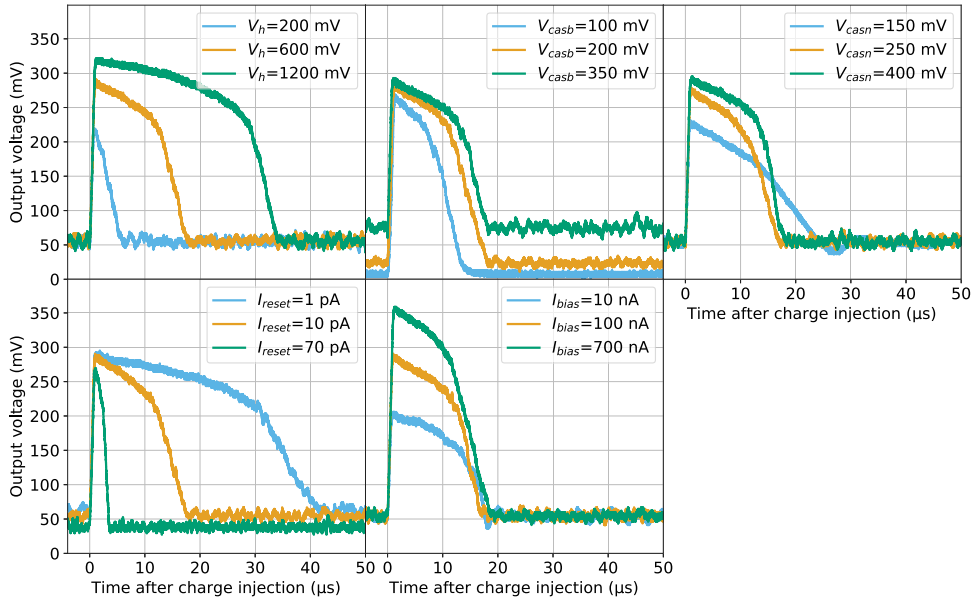


Fig. 5. The analogue responses produced when the monitor pixel is pulsed and V_h, V_{casb}, V_{casn}, I_{reset} and I_{bias} are varied. For I_{bias}, $I_{biasn} = I_{bias}/10$. Other chip bias settings not mentioned in the legend are at nominal values (cf. Section 3.1).

V_{pwell} voltage and current levels in the circuit. The power consumption in the steady state is given by the current in the main branch (I_{bias}) as the reset current is orders of magnitude lower and the I_{db} current in the discriminator branch is flowing only while M10 is active. With the typical settings used in this paper (cf. Section 3.1), it amounts to about 120 nW.

A test circuitry, which can inject charge in the collection electrode through a capacitance of $C_p = 160$ aF, is also integrated in the pixel (cf. Figs. 2 and 3). The amount of injected charge can be regulated by an external voltage reference, V_h, and the injection is triggered by asserting the TRG signal via an interface pad.

Besides the 1024 digital output pixels, the DPTS features a monitoring pixel with an analogue output connected to an interface pad. The analogue pixel front end is identical to the one described above with the exception of the last common-source stage being replaced by a source follower, which buffers its analogue output signal to the interface pad.

2.2. Hit position encoding and time-over-threshold

The transition of the discriminator output triggers the address generator (cf. Fig. 2) to send two consecutive pulses on the CML output with a duration based on the pixel position [16]. As indicated in Fig. 4, the first pulse is of a fixed duration, the time distance between the two pulses encodes the pixel position in a group of columns (PID) and the duration of the second pulse the column group position in the matrix (GID).

The assertion and the deassertion of the discriminator result in two sets of pulses, delimiting the time interval in which the front-end pulse was over the threshold (ToT). Because the front end is designed such that the pulse length is monotonically increasing with the input signal, the ToT provides information on the collected or injected charge.

As the time-encoded output of the 1024 pixels is merged to a single output line, two or more pixels firing simultaneously result in a signal collision, i.e. non-decodable output (the firing pixels' coordinates cannot be determined). In order to minimise the probability of signal collisions in case of charge sharing among neighbouring pixels, two optimisations were implemented in the encoding scheme: (1) the output signals of pixels in every other column are delayed by a fixed offset, and (2) in every other row of a column pair, the GID is swapped between the two pixels.

3. Laboratory measurements

3.1. Data acquisition setup

The laboratory and testbeam measurements used a custom-designed setup for the DPTS sensor that supplies biases and control signals to the chip. The CML and analogue outputs of the chip were recorded on an oscilloscope, with a sampling rate of 5 GS/s and a bandwidth of 500 MHz. For all the temperature sensitive measurements, in particular those involving irradiated chips, the chip temperature was controlled using a water-cooled (+20 °C) aluminium jig in thermal contact with the chip carrier card and thus the chip.

The bias settings of the chip are set to "nominal" values (defined by the design operating point) for all measurements unless otherwise stated or varied in the measurement. These settings are $V_{casb} = 300$ mV, $V_{casn} = 300$ mV, $I_{reset} = 10$ pA, $I_{db} = 100$ nA, $I_{bias} = 100$ nA, $I_{biasn} = 10$ nA, $V_h = 600$ mV (the pixel pulsing amplitude) and $V_{sub} = V_{pwell} = -1.2$ V. For irradiated sensors, the I_{reset} is increased to 35 pA to overcome the sensor leakage current. Furthermore, when adjusting V_{pwell}, the values of V_{casb} and V_{casn} are adjusted as well (cf. Section 2.1). The maximum V_{pwell} foreseen by the design is -6 V, however, in this work, the V_{pwell} is capped at -3 V as further increasing it did not improve performance, at least not in the measurements presented here.

3.2. Analogue response

The inclusion of an additional monitor pixel to the chip allows the analogue pulse of the front end to be directly measured (cf. Section 2.1). The monitor pixel was pulsed, and the output responses at different chip bias settings are shown in Fig. 5, demonstrating the influence of

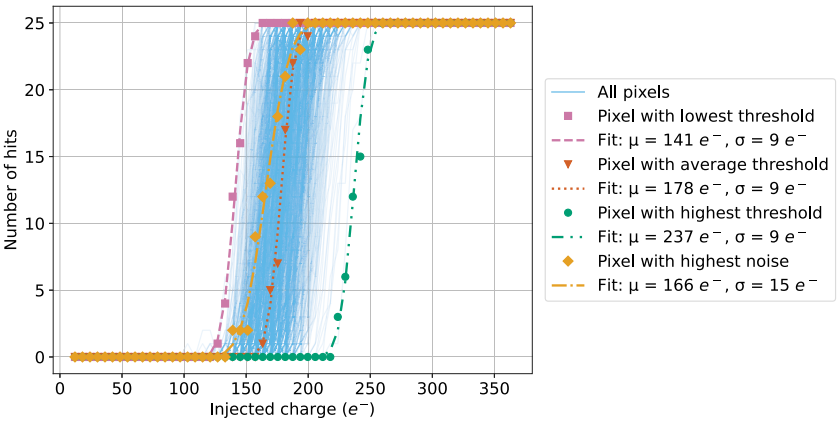


Fig. 6. S-curves of a chip tuned to a threshold of $180\,e^-$ with $V_{casb} = 180\,\text{mV}$ at $V_{sub} = -1.2\,\text{V}$. Four pixels have been highlighted along with their s-curve fits (non-solid lines). These four pixels represent the response of pixels with the lowest, average and highest threshold and the pixel with the highest noise. Other chip bias settings are at nominal values (cf. Section 3.1).

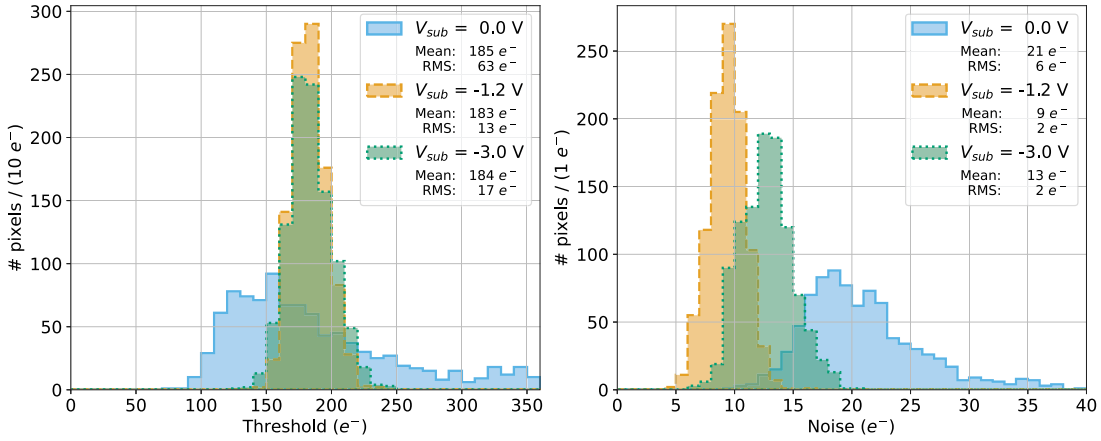


Fig. 7. Pixel threshold (left) and noise (right) distributions of a chip tuned to a threshold of $180\,e^-$ with $V_{casb} = 110,\ 180$ and $500\,\text{mV}$ at $V_{sub} = 0.0,\ -1.2$ and $-3\,\text{V}$, respectively. Other chip bias settings are at nominal values (cf. Section 3.1).

varying V_h, V_{casb}, V_{casn}, I_{reset}, I_{bias} and I_{biasn}. For the case of I_{bias}, I_{biasn} was also varied, keeping $I_{biasn} = I_{bias}/10$, which is the recommended regime.

Increasing V_h, which controls the injected charge, increases the amplitude and length of the pulse. It can easily be observed that, in accordance with the amplifier design (cf. Section 2.1) the pulse length, rather than amplitude, is proportional to the amount of injected charge. V_{casb} has a direct influence on the baseline, at low V_{casn} the pulse changes shape, I_{reset} changes the duration of the pulse and increasing I_{bias} increases the amplitude. The impact of changing I_{db} on the analogue pulse is not presented as this last stage of the front end is not included in the monitor pixel.

3.3. Threshold and noise

Investigation into the front-end response of the chip used the in-pixel pulsing circuitry to conduct threshold measurements. This involved counting the number of hits while varying V_h, that is, the amount of injected charge. For every V_h value, each pixel was pulsed 25 times. As the injected charge approaches the threshold, the number of hits increases until a plateau is reached, producing a so-called "s-curve". Fig. 6 shows examples of the measured s-curves. The threshold and the noise are given by the mean and standard deviation of the derivative of the s-curve, respectively. A hit was determined to occur if at least two sets of pulses were captured by the oscilloscope, ensuring both the assertion and deassertion of the discriminator were recorded (cf. Section 2.2). The final threshold value is calibrated to electrons via a measurement of the Mn-K$_\alpha$ peak position, details of which are given in Section 3.7, and this method is used throughout the paper. This calibration is done separately for each sensor, as deviations of up to 20% of the measured injection capacitance with respect to its design value have been observed.

Examples of the pixel threshold and noise distributions at $V_{sub} = 0\,\text{V}$, $-1.2\,\text{V}$ and $-3\,\text{V}$ are shown in Fig. 7, with the V_{casb} value chosen such that the mean threshold of all pixels is $180\,e^-$. The threshold distributions show comparable performance for $V_{sub} = -1.2\,\text{V}$ and $-3\,\text{V}$, with both having a similar width and centred around $180\,e^-$. However, at $V_{sub} = 0\,\text{V}$, the distribution is wider and asymmetric – indicating a substantial pixel-to-pixel threshold spread resulting in a non-uniform response across the matrix. For the noise distributions, $V_{sub} = 0\,\text{V}$ continues to show the widest distribution, while $V_{sub} = -1.2\,\text{V}$ has a better performance in terms of a smaller mean and spread than $V_{sub} = -3\,\text{V}$, suggesting non-optimal chip biasing settings for $V_{sub} = -3\,\text{V}$. In general, even with chip biasing settings optimised for threshold and noise, a worse performance in terms of threshold spread and noise was observed when decreasing V_{sub} towards $0\,\text{V}$ or increasing it towards $-3\,\text{V}$ and above.

Fig. 8 demonstrates the effect of the chip bias settings on the threshold at $V_{sub} = 0\,\text{V}$, $-1.2\,\text{V}$ and $-3\,\text{V}$ by plotting the mean and the RMS (given by the error bars) of all pixels. For V_{casb}, it can be observed that this chip bias has the largest impact on the threshold. Also, there is a linear relationship between the mean threshold and V_{casb} in a certain range, which is larger for larger V_{sub}. This linear relationship is the motivation for using V_{casb} as the main handle to control the threshold

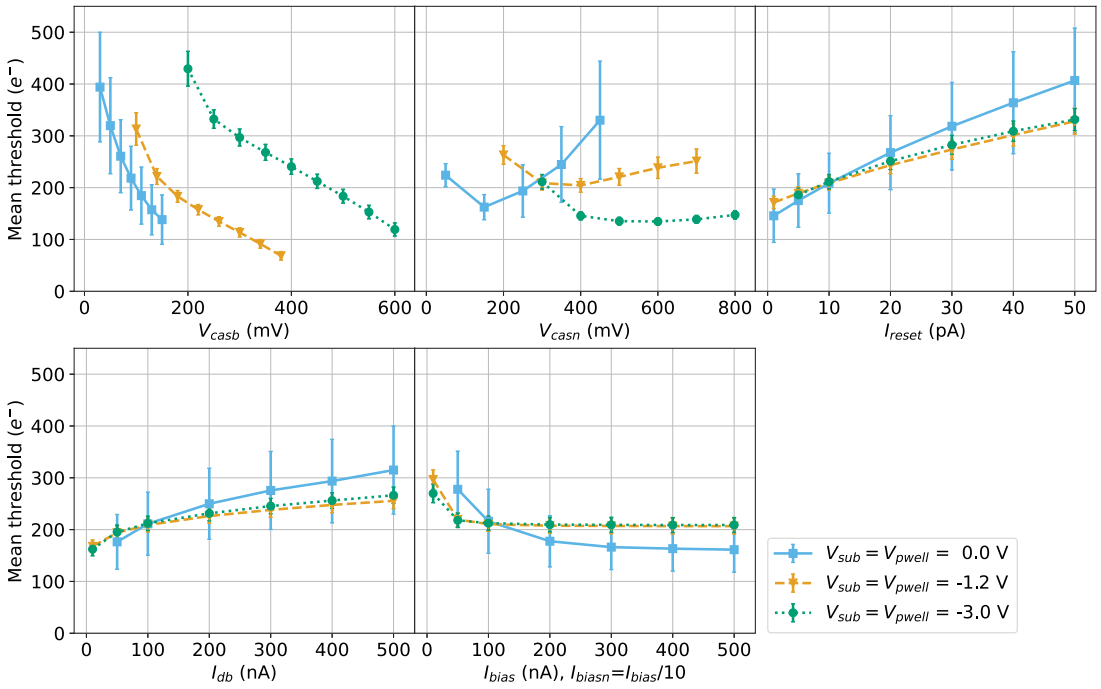


Fig. 8. The mean threshold as a function of different chip bias settings at V_{sub} of 0.0, −1.2 and −3 V with V_{casb} set to 95, 150 and 450 mV, respectively. V_{casb} was tuned so that the mean threshold was 210 e^- for nominal settings. The error bars represent the threshold RMS. The parameters not varied in the measurement are at nominal values (cf. Section 3.1).

of the chip during operation and for all subsequent results. Fig. 8 also illustrates that at different V_{sub} values, the same value of V_{casb} does not produce the same mean threshold.

While the other chip biases affect the threshold as well, for V_{casn}, I_{bias} and I_{biasn}, the influence is expected to be minimal once in a stable operating regime. The changes due to chip biases other than V_{casb} are largest at $V_{sub} = 0$ V. Whereas, at lower reverse bias values, the changes to the mean threshold (for the plotted range) are within 100 e^- except for I_{reset}, where the increase is around 150 e^-. However, this large dependence of the threshold on I_{reset} does not mean that this parameter is a good handle to set the threshold because changing I_{reset} alters the diode biasing (cf. Section 2.1) and influences the charge collection properties. Consequently, I_{reset} is only used to compensate for the increased leakage current caused by non-ionising radiation damage and not to tune the threshold.

Another operating condition that impacts the threshold is the temperature. Measurements of a non-irradiated chip have shown the mean threshold decreases by 0.5 e^- per degree Celsius in the measured range of 15–40 °C. However, for an irradiated chip, the dependence is not linear. This is compatible with the non-linear dependence of the leakage current on the temperature for higher non-ionising radiation fluence levels.

3.4. Time-over-threshold

Further investigation into the front-end response was performed by observing the impact of the chip biasing settings on the time-over-threshold (ToT, cf. Section 2.2). By varying the injected charge, Q_{inj}, and measuring the ToT for all pixels, it can be seen from Fig. 9 that at lower injected charge values, around the pixel threshold, the response is non-linear. Whereas, for larger injected charge values, the ToT response becomes linear and the spread in the ToT increases. There is also a sizeable pixel-to-pixel variation that is demonstrated by highlighting the response of two pixels. To account for this spread, a ToT calibration was performed for all pixels individually, by fitting with the empirical function

$$ToT = aQ_{inj} + b - \frac{c}{Q_{inj} - d}\ , \tag{1}$$

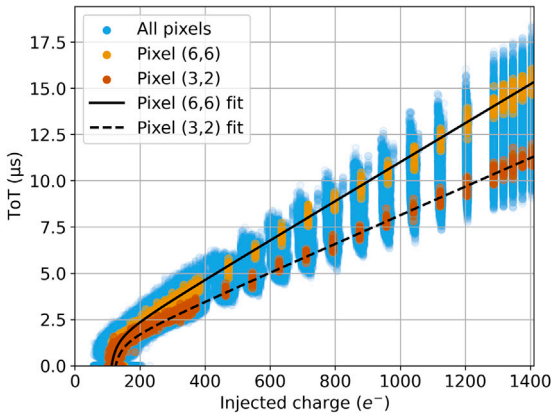


Fig. 9. Time-over-threshold (ToT) as a function of injected charge for all pixels with two pixels highlighted to demonstrate the pixel-to-pixel variation. The two pixels have been fitted with Eq. (1) shown by the solid and dashed lines.

where a, b, c and d are the fit parameters. Example fits of two pixels are shown by the solid lines in Fig. 9. The effect of the ToT calibration to normalise the pixel response over the matrix is shown and discussed in Section 3.7.

The impact of the other chip biases on ToT was also investigated at a fixed charged injection of 725 e^-. The results in Fig. 10 demonstrate that I_{reset} produces the most significant change in ToT (within 40 µs), which is compatible with I_{reset} resetting the diode (cf. Section 2.1). For the other biases, the change is within 10 µs. Furthermore, the non-linear behaviour of the ToT as a function of V_{casb} for values above 70 mV illustrates the limited operation margin at $V_{sub} = 0$ V.

3.5. Fake-hit rate

The impact of the chip bias settings on the fake-hit rate (FHR) was evaluated and is shown in Fig. 11. The FHR is defined as the number of hits per pixel and second in the absence of external stimuli as the chip operates in a continuous readout. Given that the oscilloscope captures a fixed-size time window, the FHR is estimated as the aggregate of hits

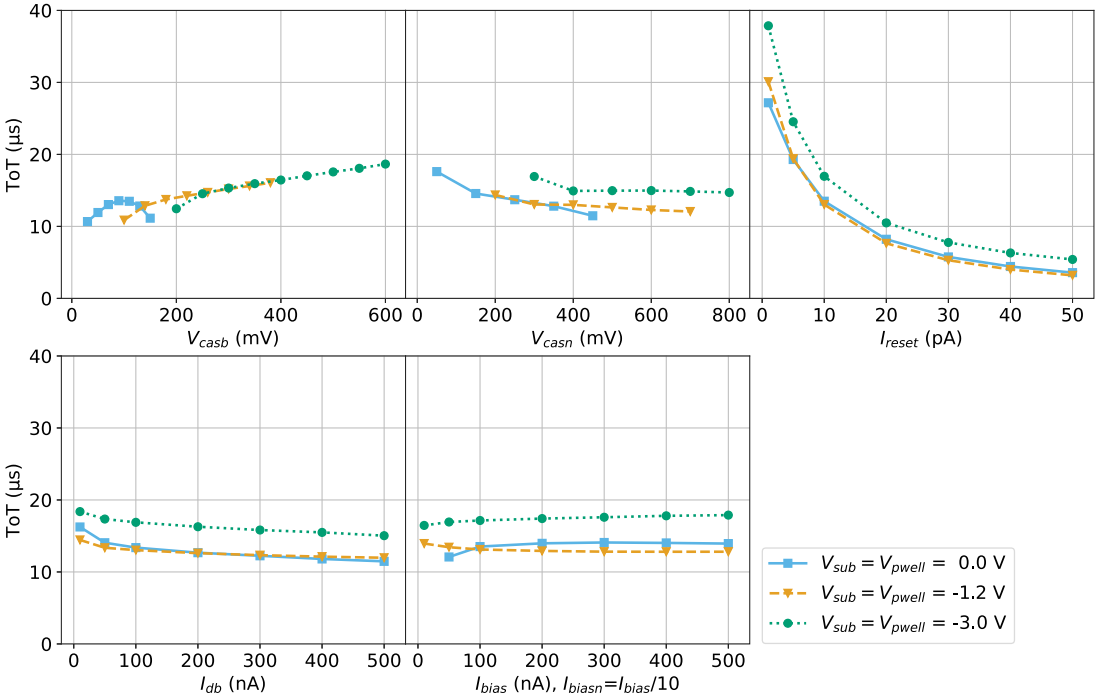


Fig. 10. Time-over-threshold (ToT) as a function of different chip biases at a fixed charged injection of $725\,e^-$. Non-varied parameters are at nominal values (cf. Section 3.1).

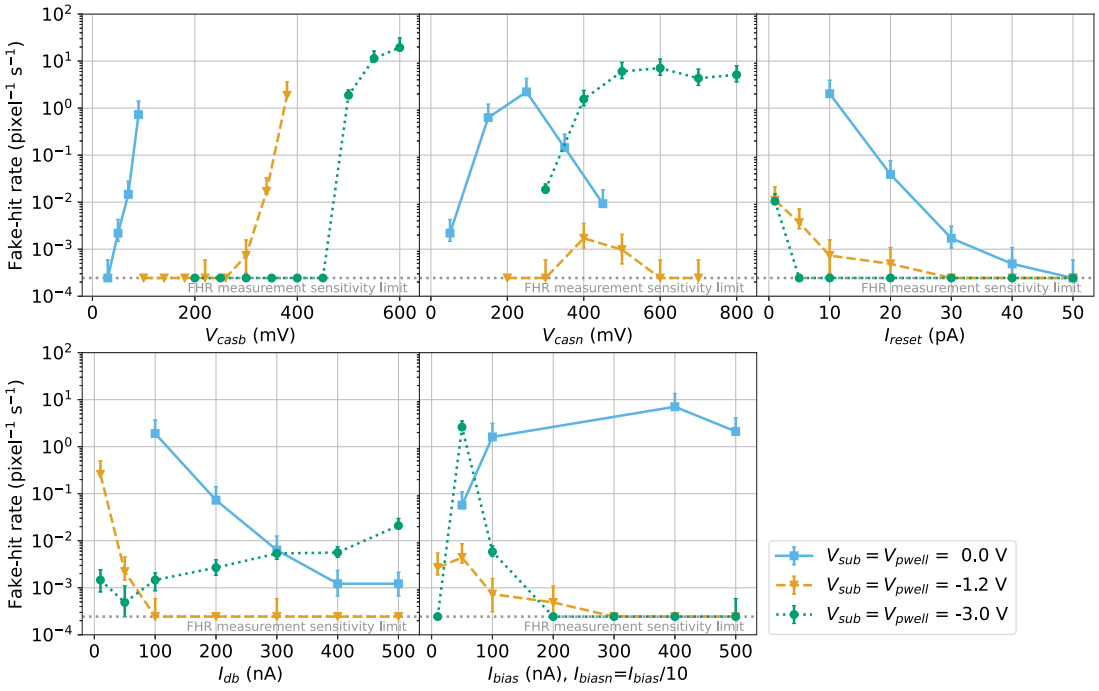


Fig. 11. Fake-hit rate as a function of different chip biases. At $V_{sub} = -1.2\,\mathrm{V}$, the threshold was set at $120\,e^-$, while for the other V_{sub} values it was $210\,e^-$ (for the nominal parameters). Other chip bias settings not varied in the measurement are at nominal values (cf. Section 3.1).

in a number of randomly triggered oscilloscope acquisitions divided by the sum of their duration and the total number of pixels (1024). In general, the measurements show that the lower the threshold, the higher the FHR. As with the threshold results shown in Section 3.3, operating at $V_{sub} = -1.2\,\mathrm{V}$ gives the best performance, with many of the results below the sensitivity limit[3] of the measurements, even at the low threshold used for the measurements. At $V_{sub} = 0\,\mathrm{V}$, the sharp increase in the FHR from the lowest operable V_{casb} further illustrates the limited operation margin without supplying reverse bias.

3.6. Pixel position decoding

As described in Section 2.2, the positions of the hit pixels are time-encoded in the CML output pulses in terms of PIDs and GIDs. An example of the measured PIDs and GIDs for all pixels, each pulsed 100 times, at $V_{sub} = V_{pwell} = -1.2\,\mathrm{V}$ and $-3\,\mathrm{V}$ is given in Fig. 12.

[3] The sensitivity limit is defined as the lowest measurable FHR for the number of oscilloscope captures in the measurement.

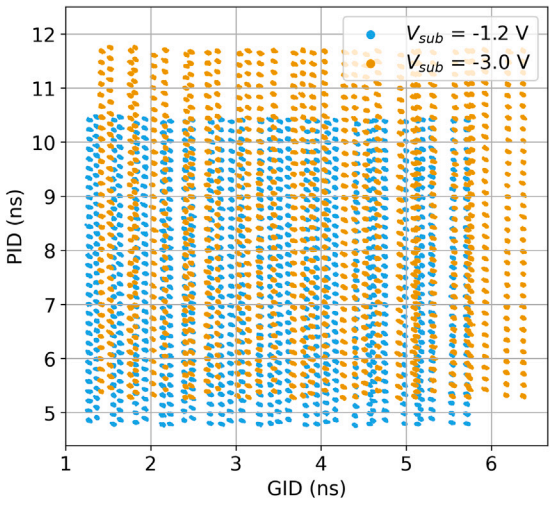


Fig. 12. The PID and GID data points corresponding to all pixels pulsed 100 times at $V_{sub} = V_{pwell} = -1.2$ V and -3 V demonstrating the reverse bias dependence. Each cluster consists of 100 points and represents the measured PID and GID value for one pixel.

It can be observed that the data points form clusters, corresponding to 1024 pixels. Some of the clusters for the different pixels are very close (and look to be overlapping due to an artefact of the axis scales), demonstrating where the decoding errors can arise.

Given that the time constants in the encoding are dependent on the production process and measurement conditions [16], a decoding calibration is needed to convert the measured PIDs and GIDs of the waveforms to pixel rows and columns. The calibration is performed by pulsing each pixel 100 times and measuring the PIDs and GIDs of the recorded waveforms. The centre of gravity of the PID and GID cluster for each pixel gives the decoding calibration. By associating a (GID, PID) pair to the nearest centre of gravity, the conversion to columns and rows is obtained.

Except for the reverse bias dependence, PIDs and GIDs were found to also depend on supply voltage and temperature. In particular, it was found that the mean PID and GID increase by 8 ps and 4 ps per degree Celsius, respectively, in the range 15–40 °C.

3.7. Measurements with X-rays emitted by an ^{55}Fe source

X-ray emissions from an ^{55}Fe source illuminating the top side of the chip at a distance of approximately 12 mm have been measured. Two cuts have been applied to the data: the removal of all pixels on the matrix edge and the removal of pixels with hit rates of five standard deviations above the mean. The measured signal spectrum of clusters involving only one pixel for a sensor with a threshold tuned to 120 e^- is shown in Fig. 13 (in blue).

A ToT calibration for each pixel is applied to account for the variation in the pixel-to-pixel response, as described in Section 3.4. After the ToT calibration, the Mn-K$_\alpha$ and Mn-K$_\beta$ emission peaks are resolved, as shown in Fig. 13 (in orange), as well as the Mn-K$_{\alpha,\beta}$ escape (Mn-K$_{\alpha,\beta}$ − Si-K$_{edge}$) and silicon fluorescence (Si-K$_{\alpha,\beta}$) peaks. The Mn-K$_\alpha$ and Mn-K$_\beta$ peaks are fitted with a sum of two Gaussians. The resolution of the Mn-K$_\alpha$ peak is defined as the FWHM divided by the measured peak value and was calculated to be (7.42 ± 0.01)%. For the fluorescence and escape peaks, the signal is fitted with a Gaussian and a background fit of either exponential or linear form for the fluorescence and escape peaks, respectively. Since the response of ToT as a function of injected charge was found to be linear for ToT values above 3 μs (cf. Section 3.4), the comparison between the measured and literature peak values is fitted with a linear function, giving the conversion from ToT to energy in e^-.

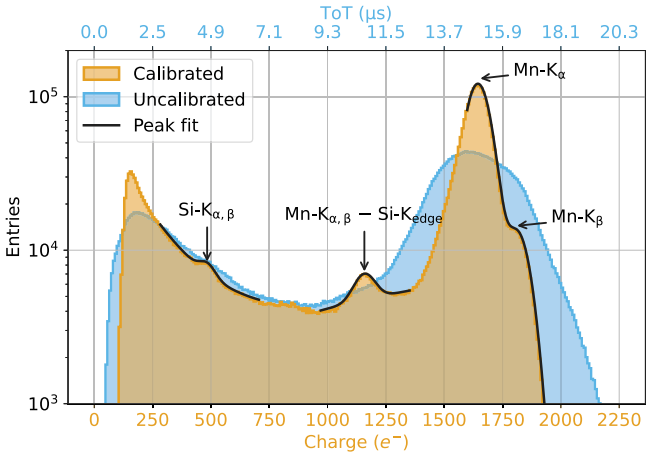


Fig. 13. Measured ^{55}Fe spectrum of single pixel clusters with a threshold set to 120 e^-. The initial spectrum (blue) is ToT calibrated (orange) which resolves the two x-ray peaks (Mn-K$_\alpha$ and Mn-K$_\beta$) plus the Mn-K$_{\alpha,\beta}$ escape (Mn-K$_{\alpha,\beta}$ − Si-K$_{edge}$) and silicon fluorescence (Si-K$_{\alpha,\beta}$) peaks.

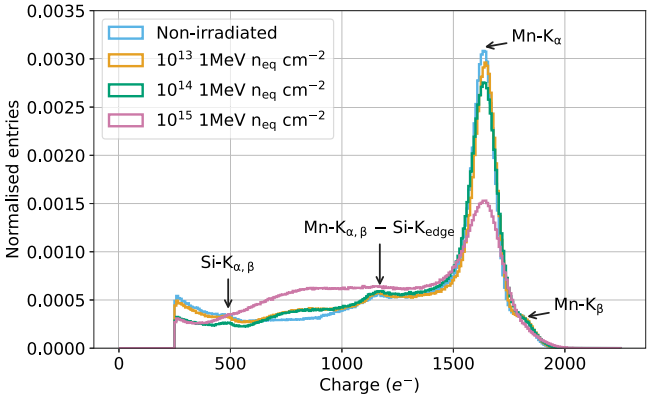


Fig. 14. Measured ^{55}Fe spectra of seed pixels for different levels of non-ionising irradiation: non-irradiated, 10^{13}, 10^{14} and 10^{15} 1 MeV n_{eq} cm^{-2}.

Table 1
Measured resolution of the Mn-K$_\alpha$ peak for different levels of non-ionising irradiation in seed pixel signal spectra in Fig. 14.

Irradiation	Resolution (%)
Non-irradiated	7.40 ± 0.02
10^{13} 1 MeV n_{eq} cm^{-2}	7.42 ± 0.03
10^{14} 1 MeV n_{eq} cm^{-2}	8.73 ± 0.02
10^{15} 1 MeV n_{eq} cm^{-2}	12.05 ± 0.07

Fig. 14 shows the measured ^{55}Fe spectra for sensors irradiated with different non-ionising doses (non-irradiated, 10^{13}, 10^{14} and 10^{15} 1 MeV n_{eq} cm^{-2}). For these measurements, the seed pixel ToT is plotted, where the seed pixel is defined as the pixel with the largest ToT in the set of adjacent pixels firing within the same oscilloscope capture. As the level of irradiation increases, the Mn-K$_\alpha$ peak becomes broader, with a notable broadening between 10^{14} 1 MeV n_{eq} cm^{-2} and 10^{15} 1 MeV n_{eq} cm^{-2}. These differences are shown in the resolution of the Mn-K$_\alpha$ peak between the irradiated sensors whose values are given in Table 1. The table shows that the largest increase in the resolution is from 10^{14} 1 MeV n_{eq} cm^{-2} to 10^{15} 1 MeV n_{eq} cm^{-2}. In addition, at the largest irradiation dose, the four peaks are no longer resolved and the contribution from seed pixels with energy in the range of 400–1400 e^- becomes more prominent. These changes to the spectrum at 10^{15} 1 MeV n_{eq} cm^{-2} indicate an alteration to the charge collection mechanisms in the sensor due to radiation damage, such as the increased recombination rate and the changes in the electric fields.

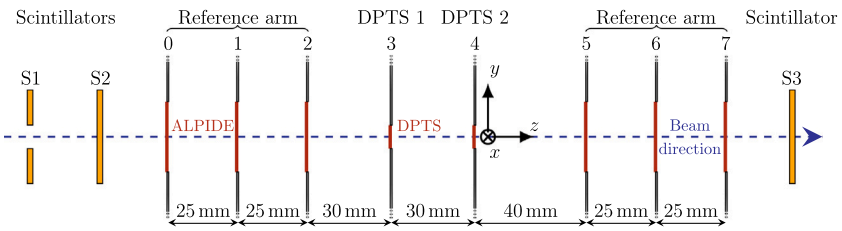


Fig. 15. Sketch of the beam telescope (not to scale). Two DPTS are sandwiched between reference planes comprised of ALPIDE chips. Two scintillators (S2 and S3), operated in coincidence, and one featuring a 1 mm hole (S1), operated in anti-coincidence, are used for triggering. The trigger can also be provided by one of the two DPTS.

4. Measurements with ionising particle beams

The DPTS sensors were also characterised at facilities providing charged particle beams. The results presented in this section are based on data taken from September 2021 to July 2022 at DESY II [17] and CERN PS testbeam facilities. As such, the sensors were subject to normally incident 5.4 GeV/c electrons and 10 GeV/c positive hadrons, respectively.

4.1. Setup

A beam telescope comprising of reference planes equipped with ALPIDE chips [4–6] has been used to reconstruct particle tracks. Two DPTS sensors were installed in-between the reference planes. A sketch of the beam telescope is shown in Fig. 15. The data acquisition was based on the EUDAQ2 framework [18]. The trigger signal was provided either by one of the DPTS chips or by a discriminated output of photomultiplier tubes (operated in the plateau regime) connected to a set of three 2 cm × 2 cm scintillators placed in front and behind the telescope. One of the scintillators (S1) features a 1 mm hole in its centre and is operated in anti-coincidence with the other two ($\neg$S1 $\wedge$ S2 $\wedge$ S3, cf. Fig. 15). The x and y position of a DPTS and the anti-coincidence scintillator were adjustable via micro-positioning stages to achieve the overlap with the other DPTS. The DPTS chip(s) not used for triggering are the device(s) under test or DUT(s). An aluminium cooling jig (cf. Section 3.1) with a 1 mm opening corresponding to the chip position was used to keep the DUT at a controlled temperature of +20 °C during the detection efficiency and position resolution measurements.

4.2. Analysis tools and methods

Data were processed in the Corryvreckan test beam reconstruction software framework [19] by fitting General Broken Lines [20] to clusters found in the reference planes and interpolating the tracks to the DUT(s). Event and track quality selection criteria were applied to ensure a clean data sample: precisely one track per event, reduced track $\chi^2 < 3$, and track points on each reference plane. Pixels on the reference planes with too large hit-rate (more than 1000 times the average; <1 pixel per plane were affected) were masked. Furthermore, the tracks intersecting the DUT within two pixel pitches from the sensor edge were rejected.

The DPTS hit pixel position was derived from the CML output corresponding to the assertion of the in-pixel discriminator (cf. Section 2.2). The non-decodable events, resulting from the collisions on the CML lines when multiple pixels fire simultaneously, were associated to pixel (15, 15), i.e. to the centre of the matrix. Given the negligible likelihood that two fake hits coincide in time and result in a non-decodable event, these events are considered as real hits with an undetermined position. The fraction of such events was below 3%, for all chips and settings.

In the detection efficiency calculation, the DUT clusters were associated to tracks passing within a circular window with a radius of 480 µm. The loose spatial cut prevents the underestimation of the efficiency that would result from the exclusion of non-decodable events associated to pixel (15, 15). In order to minimise the probability of associating a fake (noise) hit to a track, the DUT response was required to be within 1.5 µs of the trigger signal. The efficiency of the DUT is then estimated by the fraction of tracks with associated clusters. The relative uncertainties are obtained by calculating the 68.3% Clopper–Pearson confidence interval and summing in quadrature the probability of associating a fake hit (given by the in-situ measured fake-hit rate, cf. Sections 3.5 and 4.3).

For the position resolution evaluation, a spatial acceptance window with a radius of 45 µm around the track and a time acceptance window of 1.5 µs were applied. The distance between the intercept on the DUT plane and the associated cluster position (given by the centre of mass of pixels in the cluster) in column and row direction is determined for each track, yielding two spatial residual distributions. By fitting the latter with two Gaussian functions, the standard deviation parameters σ_{col} and σ_{row} are obtained. The position resolution is then retrieved by quadratically subtracting the estimated telescope tracking resolution of $\sigma_{track} = 2.4$ µm [21]. Given that the obtained position resolution in the two directions is equal within the measurement precision and compatible with square pixel geometry, their average will be referred to as the position resolution in the rest of the paper.

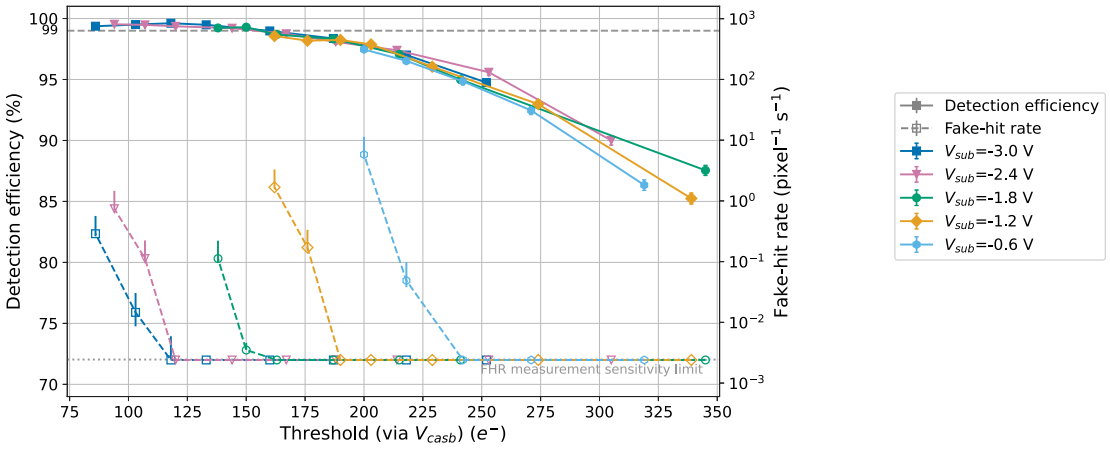
The timing resolution analysis involved no time acceptance window, while the spatial acceptance window was the same one used in the position resolution analysis.

4.3. Detection efficiency and fake-hit rate

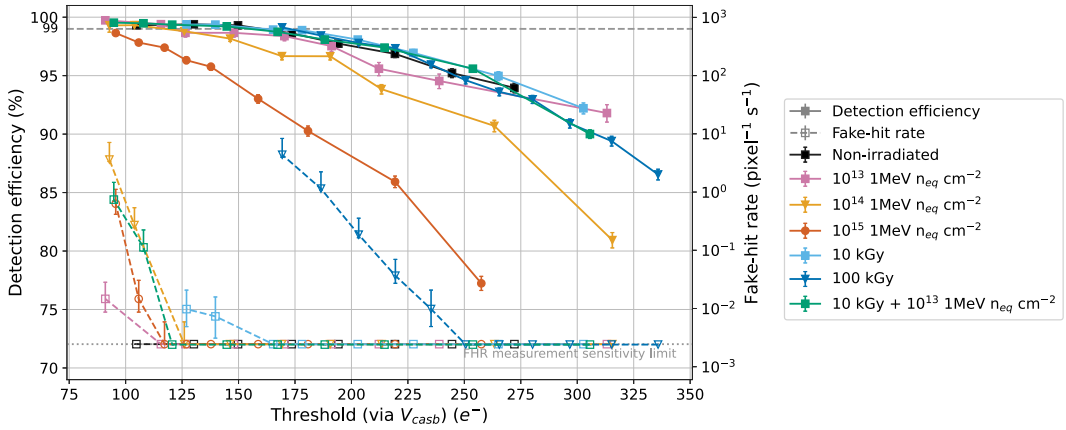
Fig. 16(a) shows the detection efficiency and the fake-hit rate (measured in situ) as a function of the average chip threshold set by changing V_{casb} at different reverse biases for a sensor irradiated with protons, i.e. that has received a combination of an ionising dose of 10 kGy and a non-ionising dose of 10^{13} 1 MeV n_{eq} cm^{-2} (levels compatible with the ITS3 requirements). Instead of showing the data for a non-irradiated sensor, which exhibits fake-hit rates below the measurement sensitivity limit, this particular sensor was chosen to better illustrate the effect of the reverse bias on the performance. In particular, it can be observed that by increasing $V_{sub} = V_{pwell}$, the onset of the measured fake-hit rate is offset to lower thresholds, thus increasing the operational margin at above 99% detection efficiency.

The effect of different irradiation levels on the detection efficiency and the fake-hit rate is shown in Fig. 16(b), where the reverse bias is kept at −2.4 V. It can be observed that non-ionising irradiation leads to a decrease in the detection efficiency, while ionising irradiation leads to an increase in the fake-hit rate. These trends are consistent with the expectation that the largest effect of the non-ionising and ionising radiation damage is on the charge collection and the noise (front-end) performance, respectively. For the 100 kGy irradiated sensor, a significant increase in the fake-hit rate can be noticed, with onset at a much higher threshold than in the other cases. Finally, although the 10^{15} 1 MeV n_{eq} cm^{-2} irradiated sensor shows notable performance deterioration, it can still be operated at 99% efficiency at the temperature of +20 °C.

The origin of the detection efficiency loss was investigated by studying its dependency on the particle hit position within a pixel. Fig. 17 shows the detection efficiency of a 10^{15} 1 MeV n_{eq} cm^{-2} irradiated sensor as a function of reconstructed track position relative to



(a) Sensor irradiated to a dose of 10 kGy and 10^{13} 1 MeV n_{eq} cm^{-2} at different $V_{sub} = V_{pwell}$.



(b) Sensors irradiated to different levels.

Fig. 16. Detection efficiency (filled symbols, solid lines) and fake-hit rate (open symbols, dashed lines) as a function of average threshold, measured with 10 GeV/c positive hadrons.

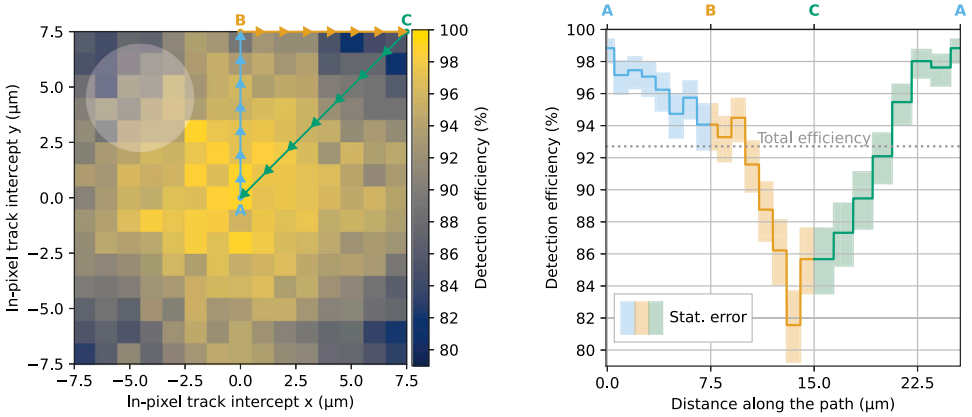
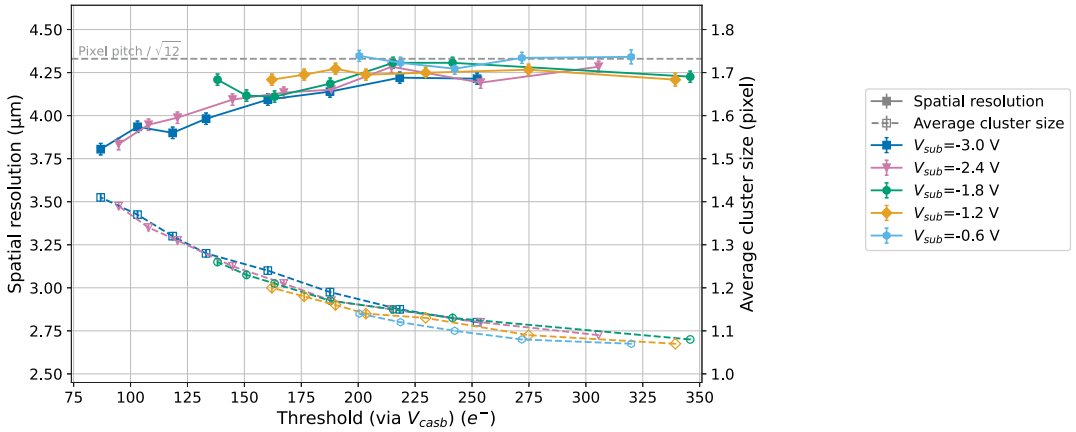


Fig. 17. In-pixel detection efficiency of a 10^{15} 1 MeV n_{eq} cm^{-2} irradiated sensor with threshold set to 160 e^-, measured with 10 GeV/c positive hadrons. The tracking resolution is represented by the white circle ($r = \sigma_{track} = 2.4$ μm) in the top left corner.

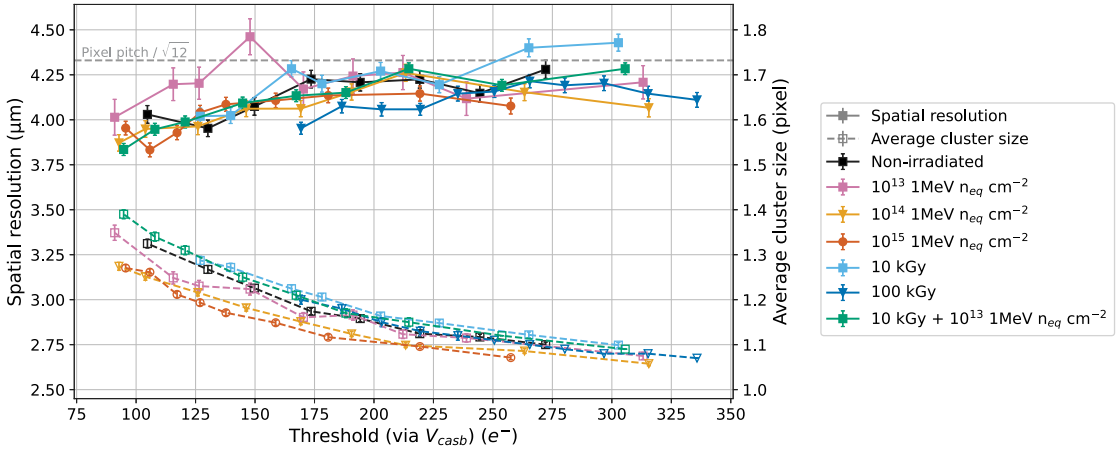
the nearest pixel centre. As expected, the detection efficiency decreases when the particle track is further away from the collection diode. A similar result was obtained for a non-irradiated sensor, with the same magnitude of efficiency loss observed at higher thresholds.

4.4. Spatial resolution and cluster size

Fig. 18(a) shows the sensor spatial resolution and average cluster size as a function of the average threshold for different V_{sub} applied, measured with 10 GeV/c hadrons for the device irradiated with both an ionising radiation dose of 10 kGy and a non-ionising radiation dose of 10^{13} 1 MeV n_{eq} cm^{-2} (levels compatible with the ITS3 requirements). The benefit of applying higher V_{sub} is not evident without combining the information from Fig. 16(a), which shows that higher V_{sub} is necessary to operate at lower thresholds. In this regime, the additional positional information, given by a larger average cluster size, results in a spatial resolution better than that of a purely binary sensor (pixel pitch divided by $\sqrt{12}$).



(a) Sensor irradiated to a dose of 10 kGy and 10^{13} 1 MeV n_{eq} cm^{-2} at different $V_{sub} = V_{pwell}$.



(b) Sensors irradiated to different levels.

Fig. 18. Spatial resolution (solid lines) and average cluster size (dashed lines) as a function of the average threshold, measured with 10 GeV/c positive hadrons.

The effect of different irradiation levels on the spatial resolution and the average cluster size is demonstrated in Fig. 18(b), where the reverse bias is kept constant at −2.4 V. Regardless of the irradiation level, the measured spatial resolution is equal or even slightly better than pixel pitch divided by $\sqrt{12}$, with no degradation of the spatial resolution performance related to the received dose. The average cluster size exhibits a slight, but systematic, decrease with the increasing non-ionising radiation dose. This trend is compatible with the previous observations of a deteriorated charge collection process.

4.5. Timing resolution

The timing resolution was estimated by measuring the output signal coincidence of two DPTS using a 5.4 GeV/c electron beam. The trigger signal and thus the time reference is given by the scintillators signal (cf. Fig. 15).

Fig. 19 (top), shows the correlation of the signal arrival time and ToT, i.e. signal amplitude, for one of the two DPTS chips. The influence of the chip readout scheme on the signal time response is notable at high ToT, where the distribution splits into two tails which correspond to odd and even columns (cf. Section 2.2). The correction for this effect is applied by subtracting the asymptotic value of the two tails from even and odd columns, respectively. The time walk observed for the lower input amplitude is corrected by fitting the data with the empirical function

$$\text{Signal time} = A + \frac{B}{ToT - C}\,, \tag{2}$$

where A, B and C are fit parameters, and then subtracting its value from the measured data points. The signal (arrival) time vs. ToT correlation corrected for the chip readout scheme and the time walk is shown in Fig. 19 (bottom). As intended, it can be observed that the amplitude of the time walk is reduced by a factor of about 3 and its asymmetric feature is removed. The correlation between the amplitude of the time walk and the time-over-threshold remains but was not further investigated in this study.

The distribution of time residuals, i.e. the time differences of the output of the two DPTSs is shown in Fig. 20 for non-corrected data (in blue) and with corrections discussed above applied independently for the two DPTSs (in orange). The timing resolution of a single DPTS is obtained by fitting the distribution with a Gaussian, and the fit parameter σ is divided by $\sqrt{2}$, resulting in $\sigma_t = 6.3\,\text{ns} \pm 0.1\,\text{ns}$ (stat). It is worth highlighting that this result is obtained by operating the chips at the low end of the in-pixel front-end power consumption range (i.e. nominal conditions in Section 3.1). An improvement in timing performances is expected by increasing the front-end current, namely I_{bias} and I_{biasn}.

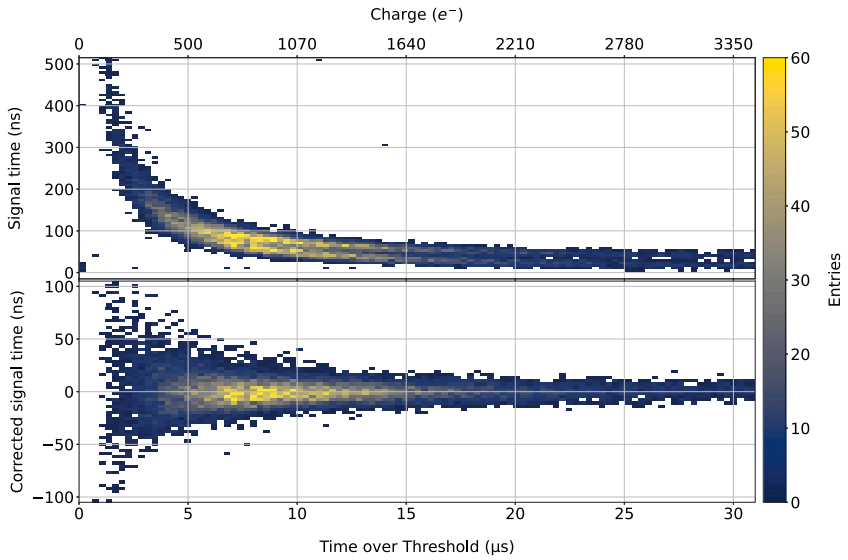


Fig. 19. Signal time vs. ToT for the upstream DPTS measured with 5.4 GeV/c electrons, with no corrections applied (top) and after readout scheme and time walk corrections (bottom). The conversion to charge is obtained by applying the procedure discussed in Section 3.7.

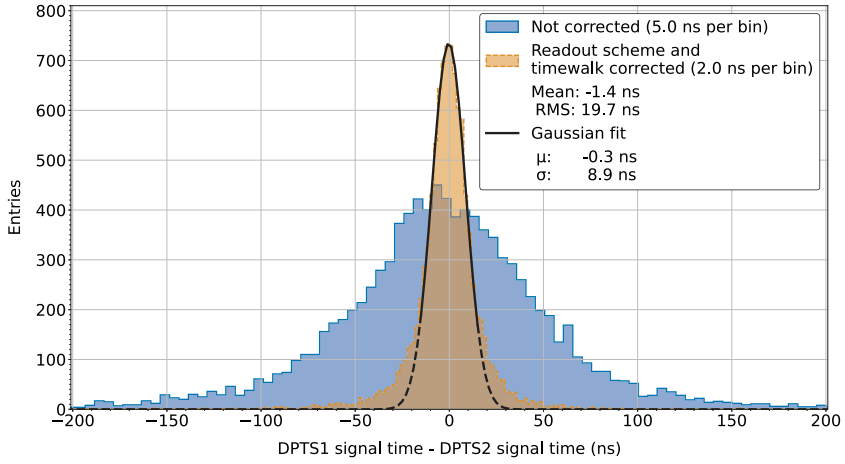


Fig. 20. Time residuals distributions of two DPTSs measured with 5.4 GeV/c electrons with no corrections (blue) and with readout scheme and time walk corrections applied (orange). The corrected distribution is fitted with a Gaussian function in the time residuals range from −15 ns to 15 ns (black solid line, dashed line for points outside the fit range).

5. Conclusions

Laboratory and in-beam measurements have been used to systematically validate the charge detection and radiation hardness of the Digital Pixel Test Structure MAPS prototype submitted in the TPSCo 65 nm process. The front end has shown a robust performance that can maintain a suitable operation regime in terms of threshold spread, noise and fake-hit rate. In addition to measuring the ToT response from X-ray emissions of an ^{55}Fe source, the DPTS achieved a resolution of $(7.40 \pm 0.02)\%$ for the Mn-K$_\alpha$ peak. The impact of irradiation on the performance becomes evident at 10^{15} 1 MeV n_{eq} cm^{-2}; however, the sensor is still able to effectively detect the X-ray emissions. This demonstration of the radiation hardness is reinforced further by the excellent detection efficiency of 99% and spatial resolution below the binary resolution for chip irradiation doses compatible with the ITS3 requirements (10^{13} 1 MeV n_{eq} cm^{-2} and 10 kGy) as well as to doses above these levels at 10^{15} 1 MeV n_{eq} cm^{-2} and 100 kGy at +20 °C while preserving a fake-hit rate below 10 pixel^{-1} s^{-1}. The DPTS also demonstrates a timing resolution of about 6 ns for the nominal chip bias settings, with improvements expected if operated at conditions optimised for timing performance.

The first step to validate this sensor technology has been presented and makes up an important aspect of the R&D for the ALICE ITS3 as well as a significant contribution to the CERN EP R&D on monolithic sensors. The excellent performance of the DPTS opens the way for further developments in this technology and with this sensor design. The next step towards a wafer-scale bent sensor and a fully cylindrical detector is the validation of stitching and yield via the full-scale sensor prototypes produced in the second submission in the 65 nm process, designated ER1.

Further work to investigate the limit of the radiation hardness of this technology and probe the performance of the DPTS with ionising particles at non-zero incident angles is foreseen. Moreover, the front-end operating point is being tuned to optimise the power consumption for low power applications, such as ALICE ITS3, where high radiation hardness and fast timing response are not crucial requirements.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

Acknowledgements

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